Evolutionary Electronics

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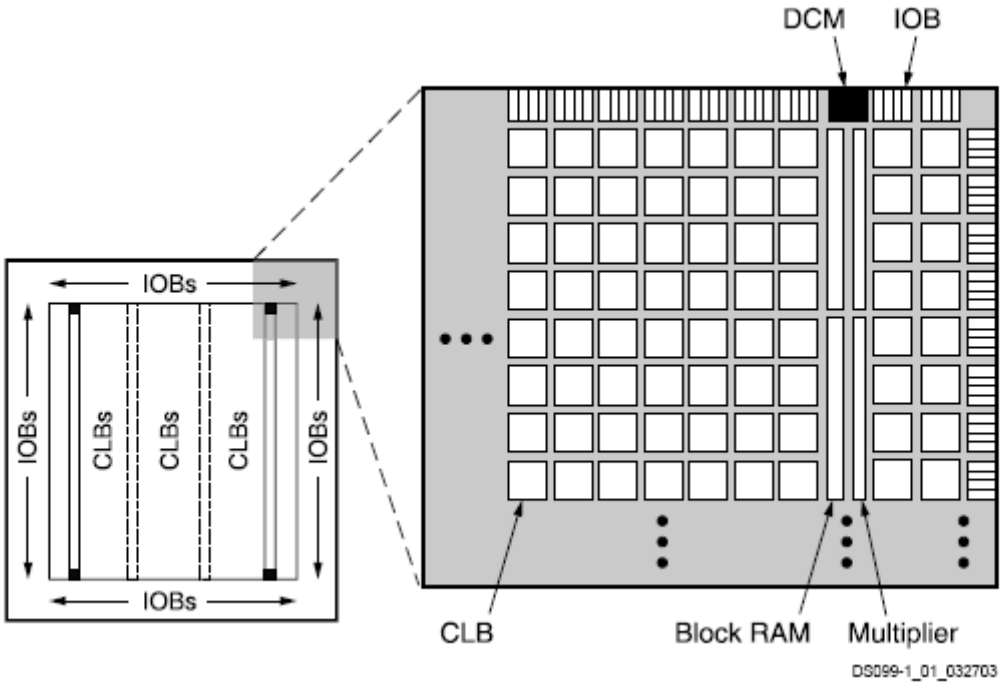
Outline

Evolutionary electronics = Reconfigurable electronics + Evolutionary Algorithms

- Reconfigurable electronics
- Evolutionary algorithms
- Early example of novel designs
- Digital design
- Evolutionary algorithm in hardware
- Other curiosities
- Current and future research

Field Programmable Gate Array (FPGA)



Spartan 3

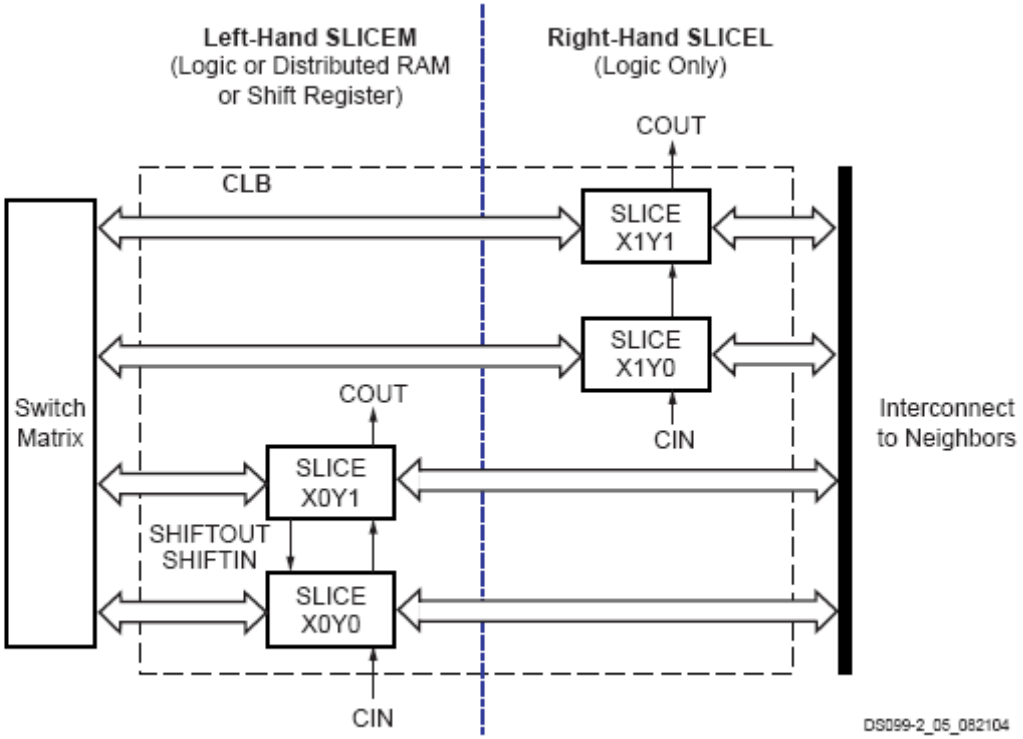
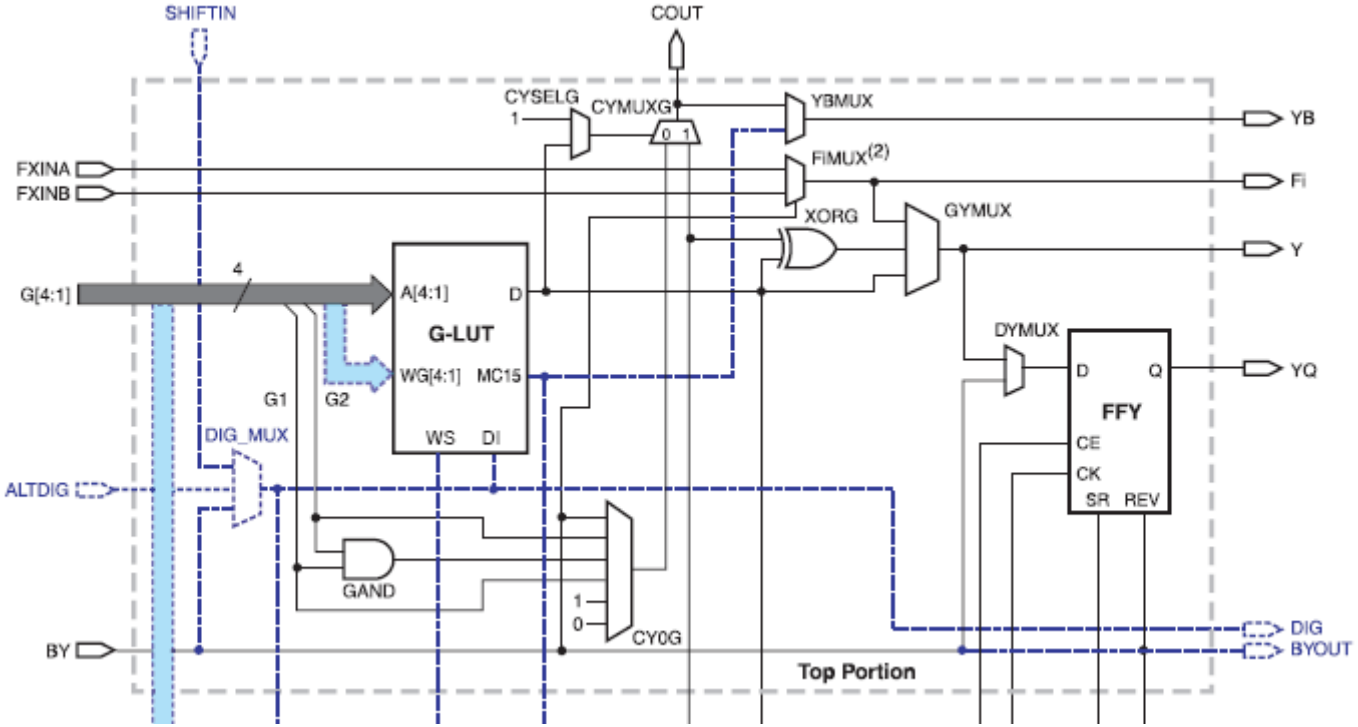
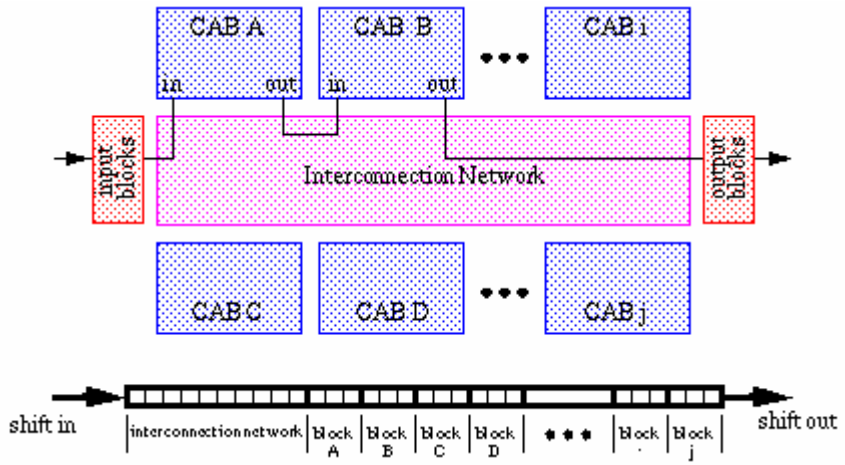


Figure 9: **Arrangement of Slices within the CLB**


SHIFTIN
COUT
CYSELG
CYMUXG
YBMUX
YB
FXINA
FXINB
FiMUX(2)
Fi
XORG
GYMUX
Y
G[4:1]
4
A[4:1]
D
G-LUT
WG[4:1]
MC15
WS
DI
DYMUX
D
Q
YQ
FFY
CE
CK
SR
REV
G1
G2
DIG_MUX
ALTDIG
GAND
CY0G
DIG
BYOUT
BY
Top Portion

Field programmable Analog Array (FPAA)

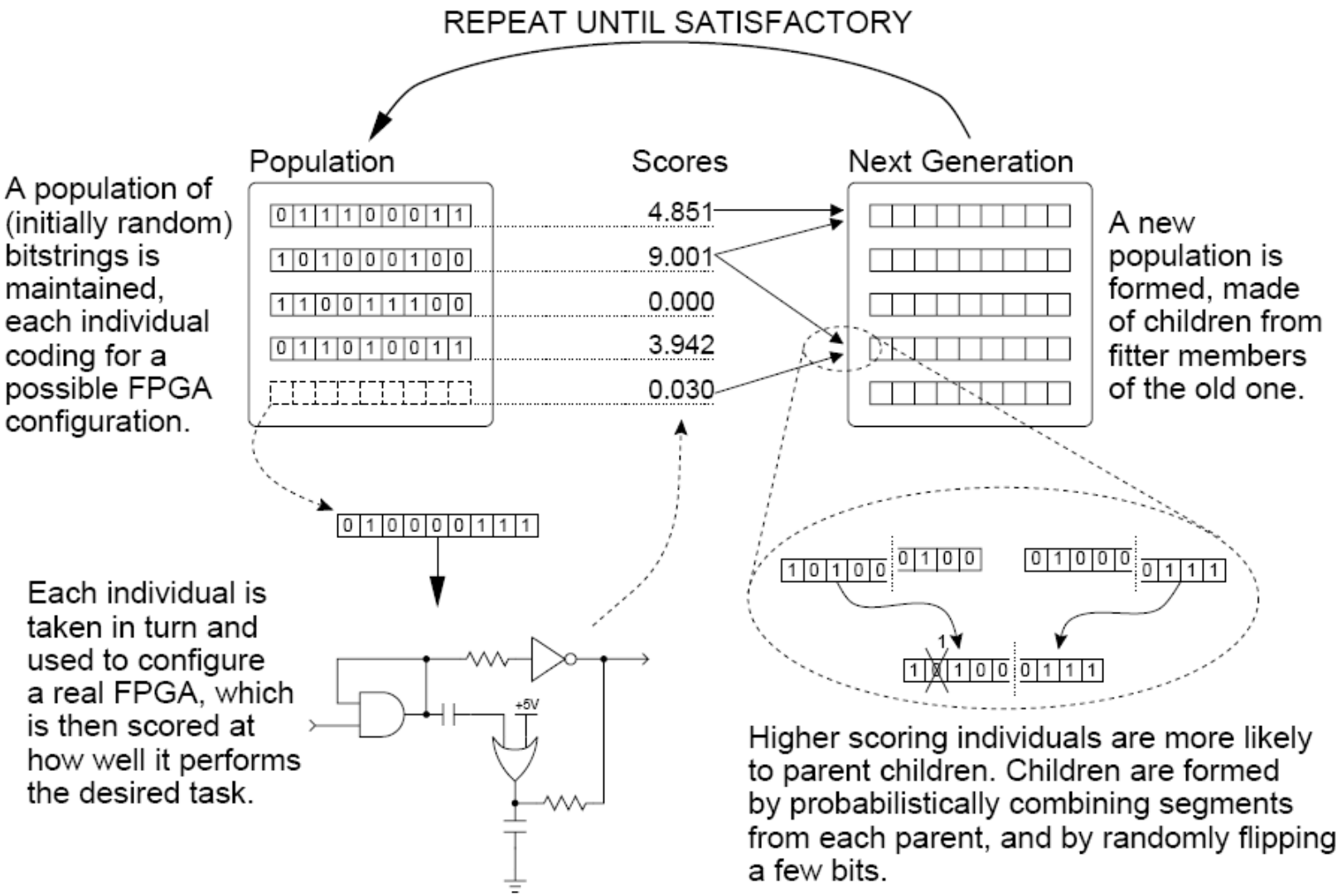


Each CAB can implement a number of analog signal processing functions such as amplification, integration, differentiation, addition, subtraction, multiplication, comparison, log, and exponential.
The interconnection network routes signals from one CAB to another, and to and from the I/O blocks.

Evolutionary Algorithms

Pool of candidates evaluate improvement

Representation of candidate: bit-string
Improvement: operation on bit-string
Bit-string represents circuits or its configuration bits


REPEAT UNTIL SATISFACTORY
Population
Scores
Next Generation
A population of (initially random) bitstrings is maintained, each individual coding for a possible FPGA configuration.
4.851
9.001
0.000
3.942
0.030
A new population is formed, made of children from fitter members of the old one.
Each individual is taken in turn and used to configure a real FPGA, which is then scored at how well it performs the desired task.
+5V
Higher scoring individuals are more likely to parent children. Children are formed by probabilistically combining segments from each parent, and by randomly flipping a few bits.

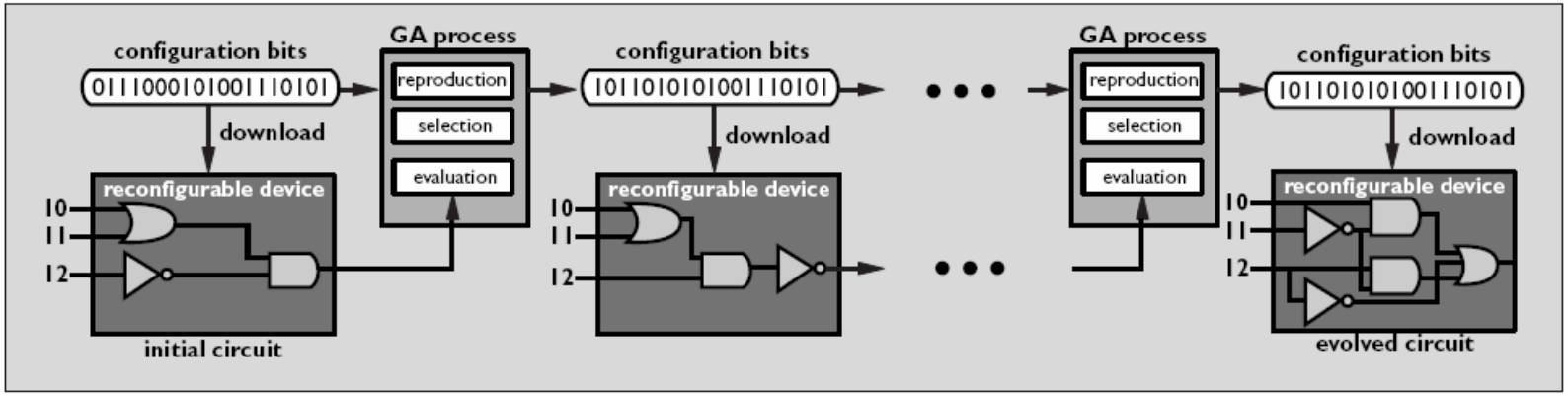


Figure 1. Basic concept of evolvable hardware.

evaluation of candidate circuits
- on-line
- off-line

circuits
- simulation
- real

evolutionary algorithms
- software
- hardware

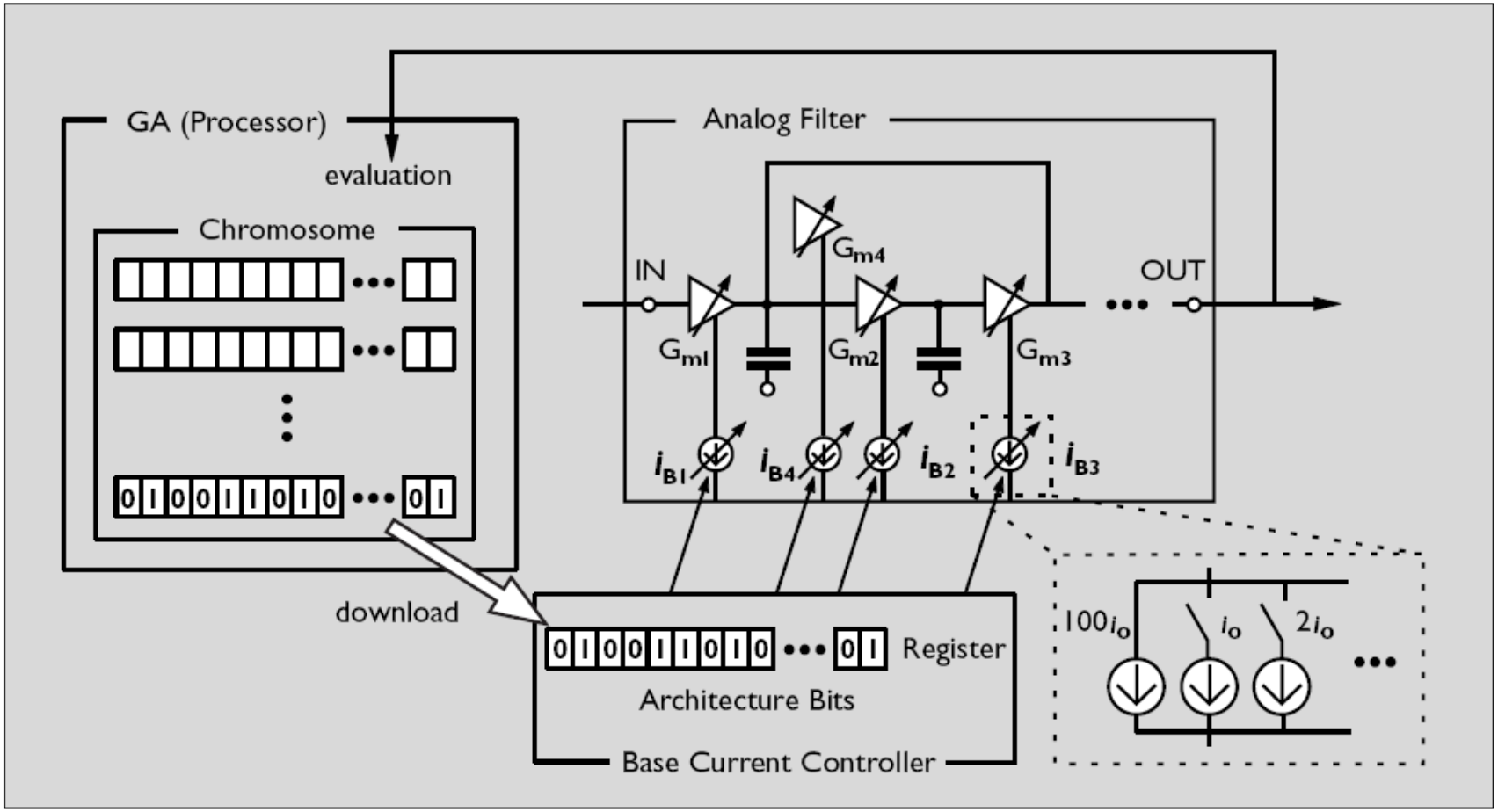


Figure 2. Basic idea of the analog EHW chip for IF filters.

(Higuchi, T. and Kajihara, N. 1999)

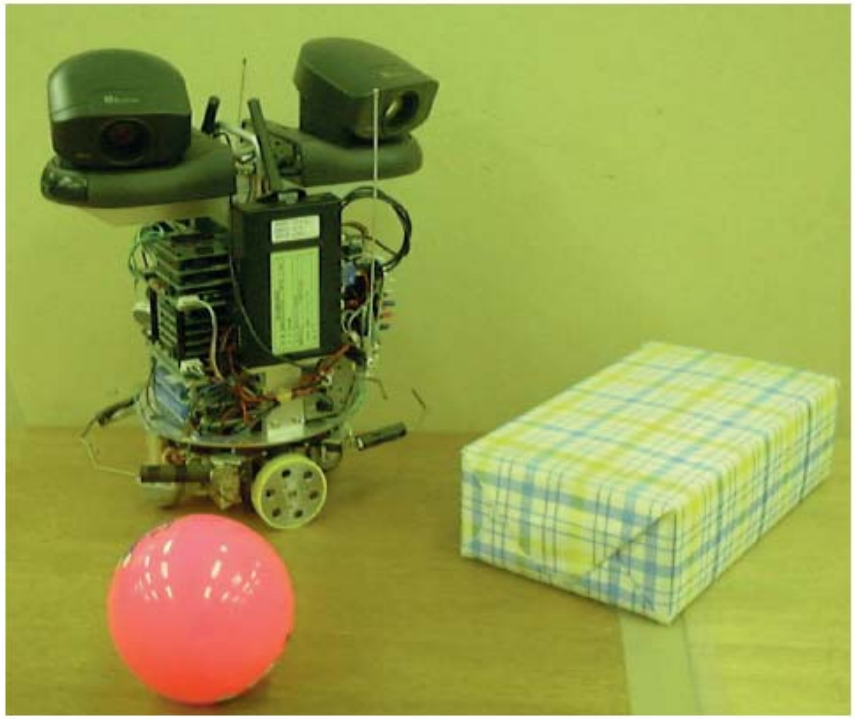
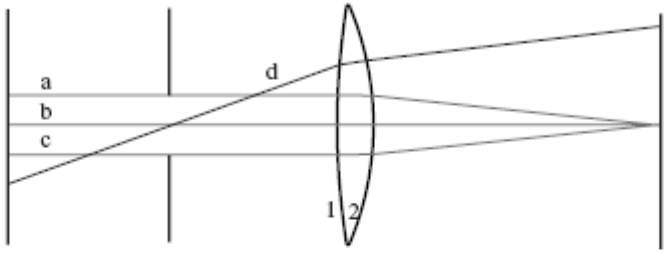
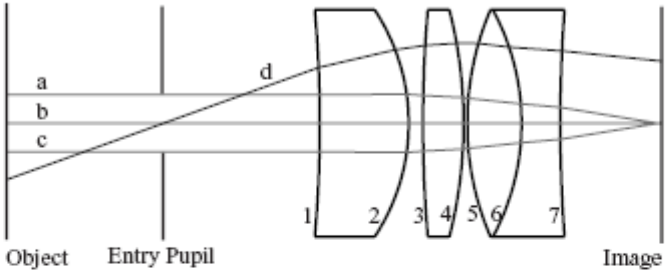
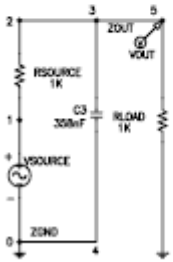
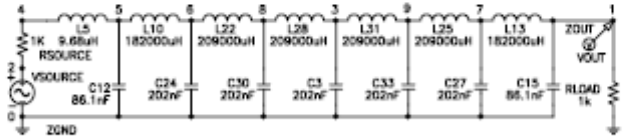


Figure 3. (left) Myoelectric prosthetic hand. **Figure 4. (right)** Autonomous mobile robot *Evolver.*

(Higuchi, T. and Kajihara, N. 1999)

Best-of-generation structure of generation 0	Best-of-run structure
 Figure 2a Optical lens system	 Figure 2b Optical lens system
 Figure 3a Lowpass filter	 Figure 3b Lowpass filter

(John R. Koza, Sameer H. Al-Sakran, Lee W. Jones 2005)

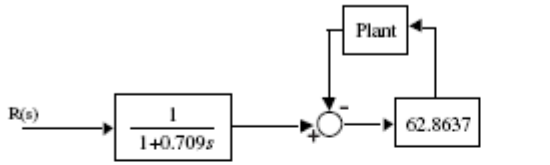


Figure 4a Controller

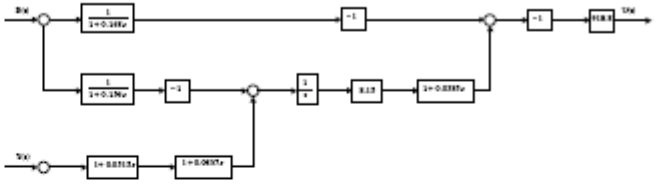


Figure 4b Controller

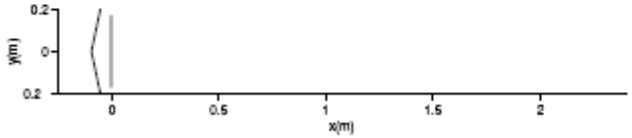


Figure 5a Antenna

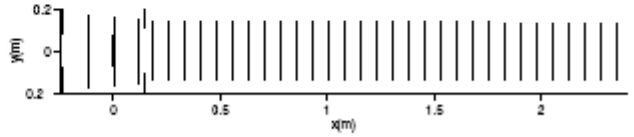


Figure 5b Antenna

(John R. Koza, Sameer H. Al-Sakran, Lee W. Jones 2005)

Invention	Date	Inventor	Place	Patent	Reference
Cubic function generator	2000	Stefano Cipriani and Anthony A. Takeshian	Conexant Systems, Inc.	U. S. 6,160,427	Section 15.4.5 of *Genetic Programming IV*
Mixed analog-digital variable capacitor circuit	2000	Turgut Sefket Aytur	Lucent Technologies Inc.	U. S.,013,958	Section 15.4.2 of *Genetic Programming IV*
Voltage-current conversion circuit	2000	Akira Ikeuchi and Naoshi Tokuda	Mitsumi Electric Co., Ltd.	U. S. 6,166,529	Section 15.4.4 of *Genetic Programming IV*
Low-voltage balun circuit	2001	Sang Gug Lee	Information and Communications University	U. S. 6,265,908	Section 15.4.1 of *Genetic Programming IV*
High-current load circuit	2001	Timothy Daun-Lindberg and Michael Miller	International Business Machines Corporation	U. S. 6,211,726	Section 15.4.3 of *Genetic Programming IV*
Tunable integrated active filter	2001	Robert Irvine and Bernd Kolb	Infineon Technologies AG	U. S. 6,225,859	Section 15.4.6 of *Genetic Programming IV*

Table 1 Six post-2000 patents for analog electrical circuits

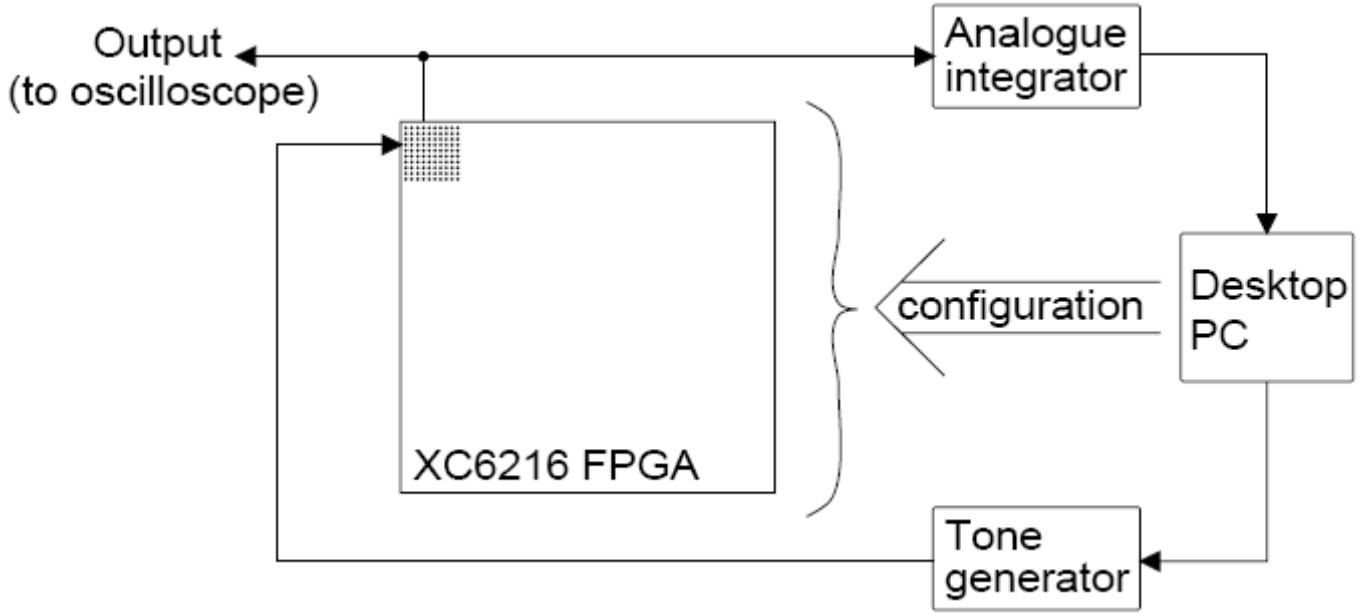
(John R. Koza, Sameer H. Al-Sakran, Lee W. Jones 2005)

Invention	Date	Inventor	Place	Patent	Reference
Telescope eyepiece	1940	Albert Konig	Carl Zeiss GmbH	U. S. 2,206,195	Al-Sakran, Koza, and Jones, 2005
Telescope eyepiece system	1958	Robert B. Tackaberry and Robert M. Muller	American Optical Company	U. S. 2,829,560	Al-Sakran, Koza, and Jones, 2005
Eyepiece for optical instruments	1953	Maximillian Ludewig	Ernst Leitz GmbH	U. S. 2,637,245	Koza, Al-Sakran, and Jones, 2005
Wide angle eyepiece	1968	Wright H Scidmore.	United States Army	U. S. 3,390,935	Koza, Al-Sakran, and Jones, 2005
Wide angle eyepiece	1985	Albert Nagler	No affiliation listed	U. S. 4,525,035	Koza, Al-Sakran, and Jones, 2005
Telescope eyepiece	2000	Noboru Koizumi and Naomi Watanabe	Fuji Photo Optical Co., Ltd.	U. S. 6,069,750	Koza, Al-Sakran, and Jones, 2005

Table 2 Six patents for optical lens systems

(John R. Koza, Sameer H. Al-Sakran, Lee W. Jones 2005)

Early Examples (on-line intrinsic)



(Thompson, A., Harvey, I., and Husbands, P., 1995)

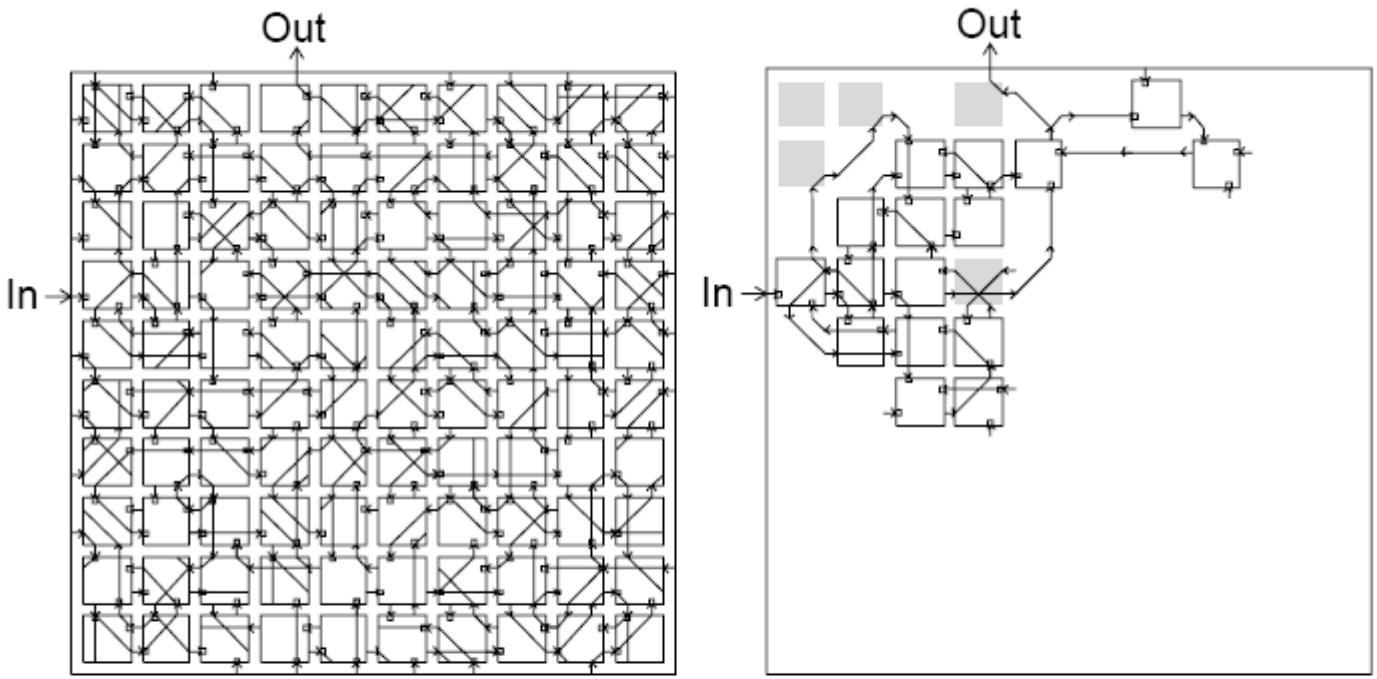
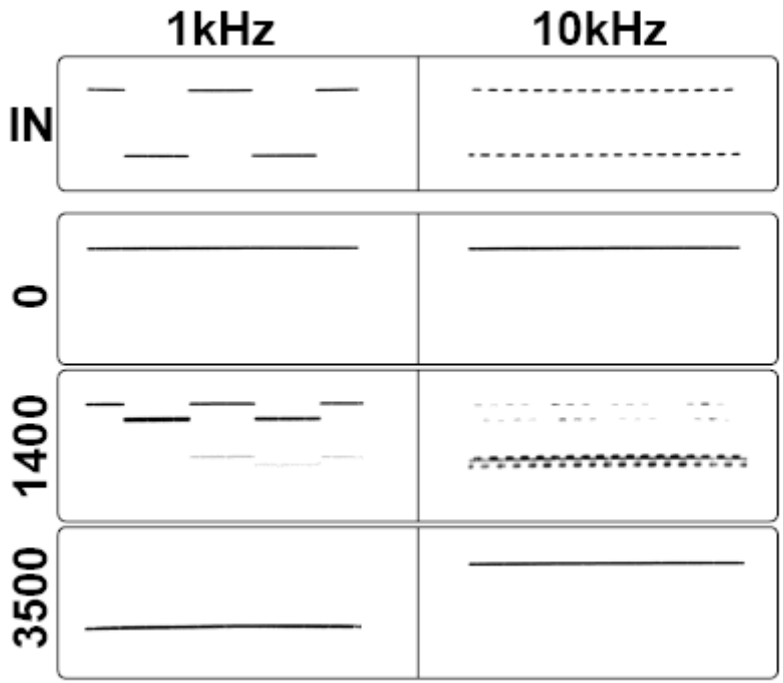


Fig. 2. On the left is shown the genetically specified configuration of the FPGA after evolution for 5000 generations. On the right is shown the subset of these connections which is functional, in the sense that the hardware still functions appropriately when the rest of the chip is clamped to fixed values.


1kHz
10kHz
IN
0
1400
3500

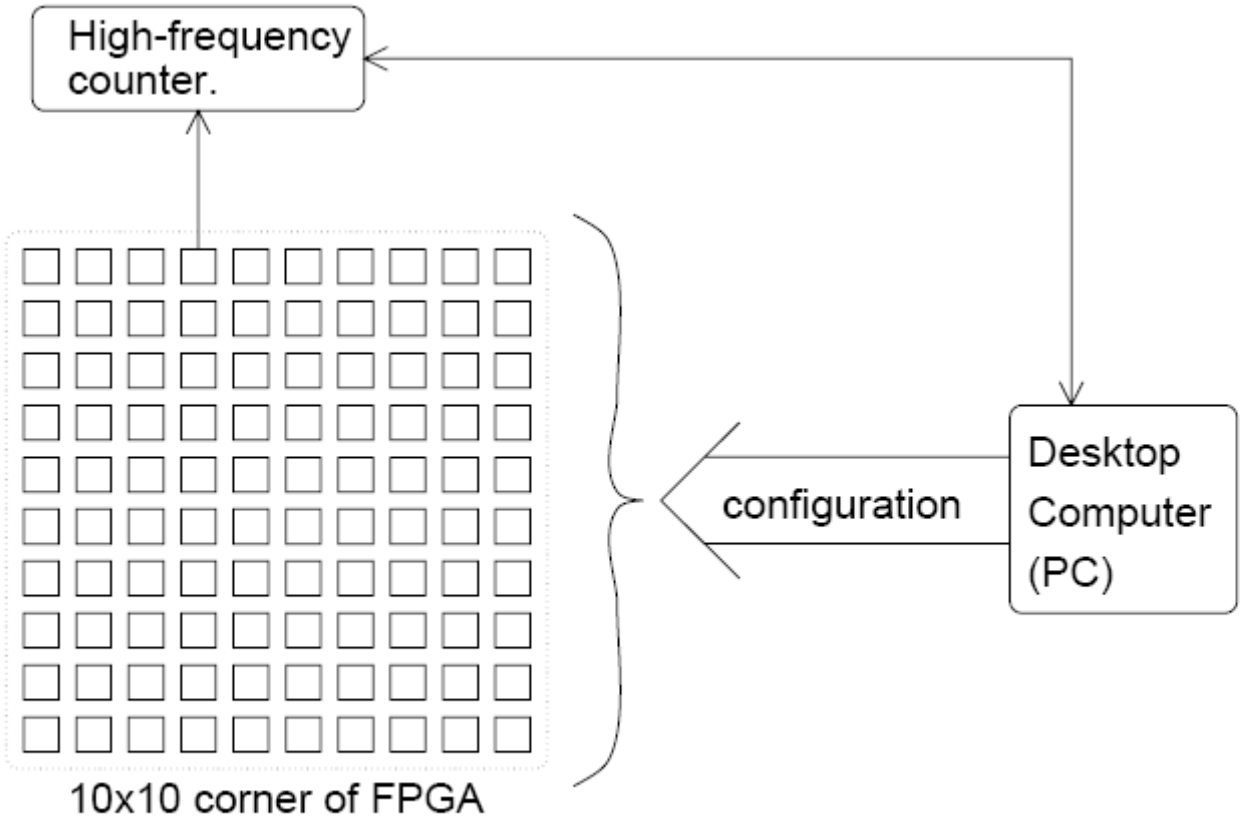


Figure 4: The experimental arrangement for oscillator evolution with the real FPGA.

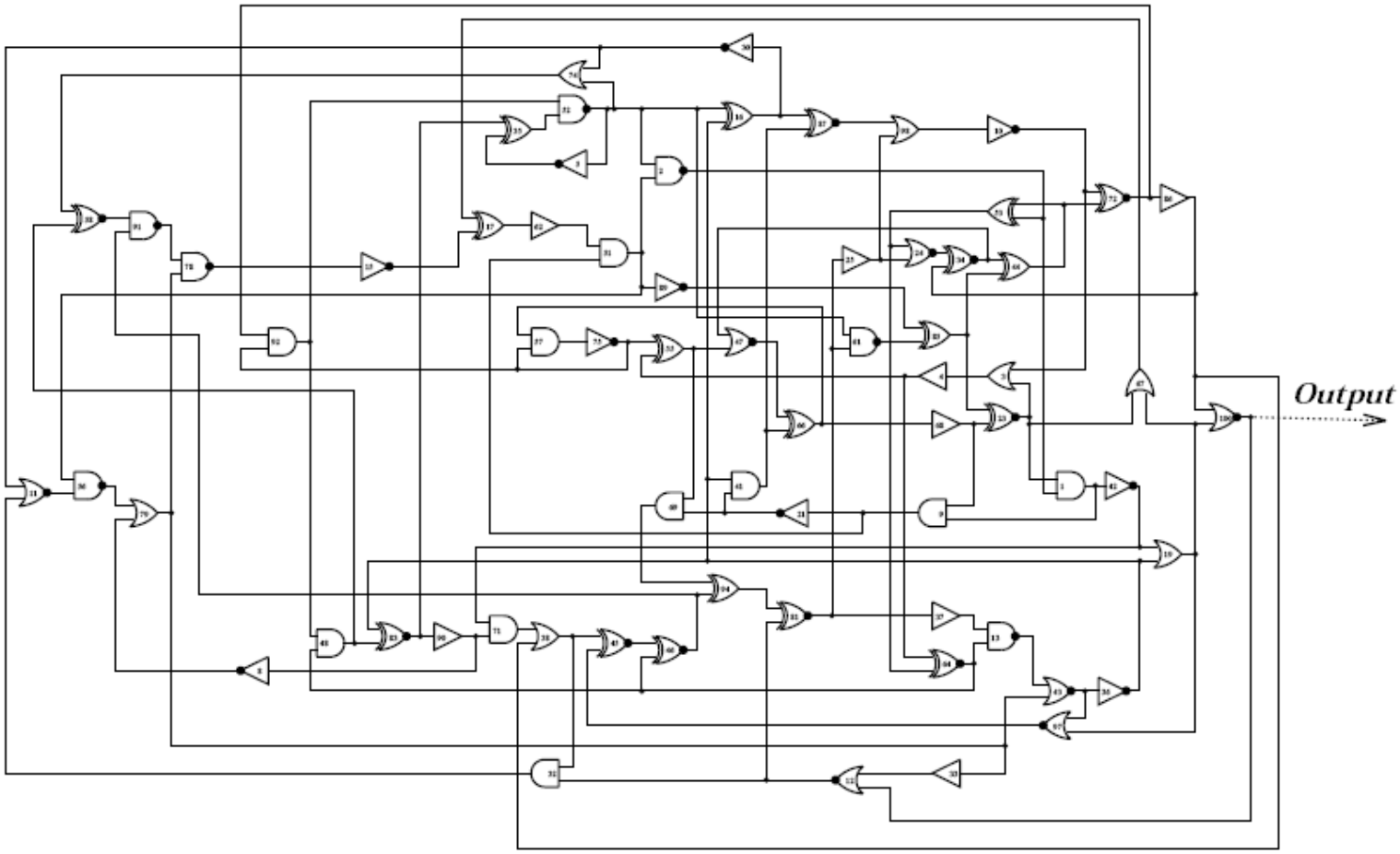


Fig. 2. The evolved 4kHz oscillator (unconnected gates removed, leaving the 68 shown).

Digital Design

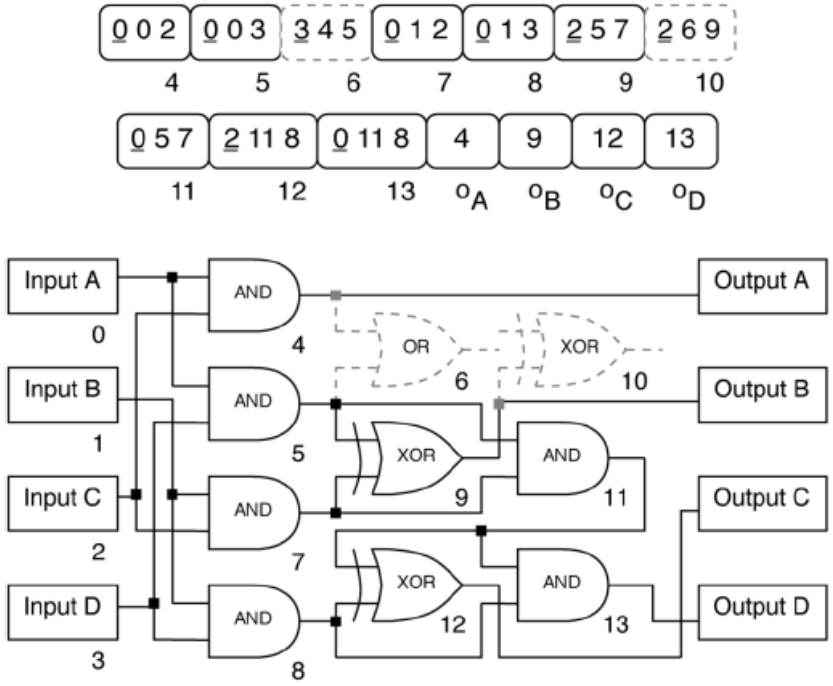
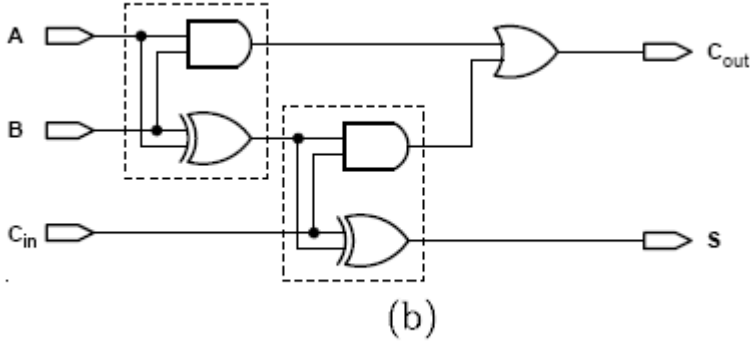


Fig. 1. A CGP genotype and corresponding phenotype for a 2-bit multiplier circuit. The underlined genes in the genotype encode the function of each node. The function lookup table is AND(0), AND with one input inverted(1), XOR(2), and OR(3). The index labels are shown underneath each program input and node in the genotype and phenotype. The inactive areas of the genotype and phenotype are shown in grey dashes (nodes 6 and 10).

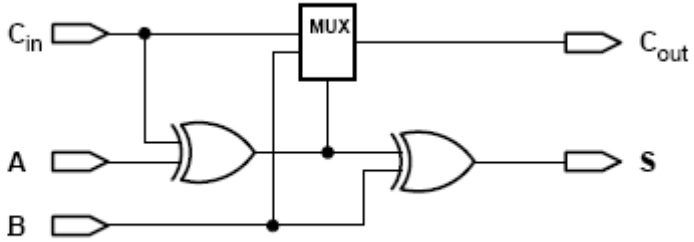
Compact Genetic Programming (CGP)
represents circuits as a feed-forward directed graph (acyclic), (Miller & Thompson, 2000)

Parity problem, adder, multiplier 2-3 bits.

Conventional one-bit adder



Evolved one-bit adder



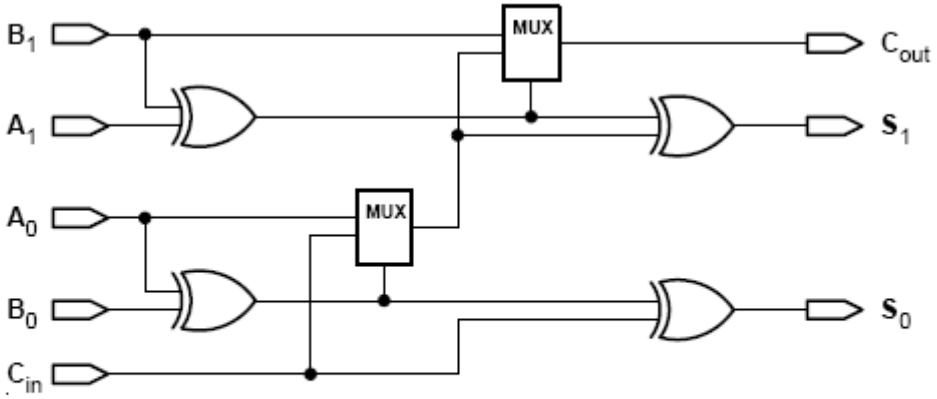


Figure 12: Evolved two-bit adder with carry.

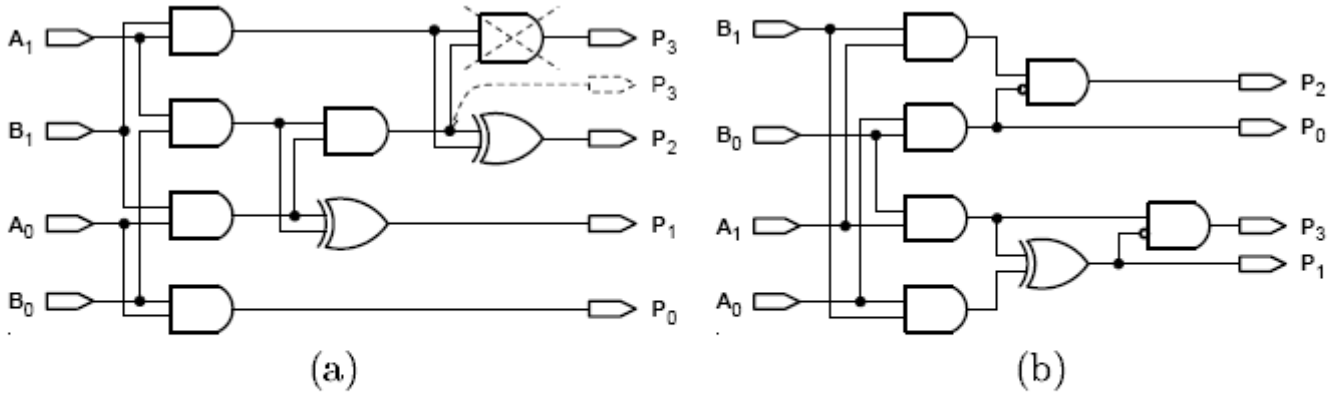


Figure 15: Most efficient (a) conventional and (b) evolved two-bit multipliers.

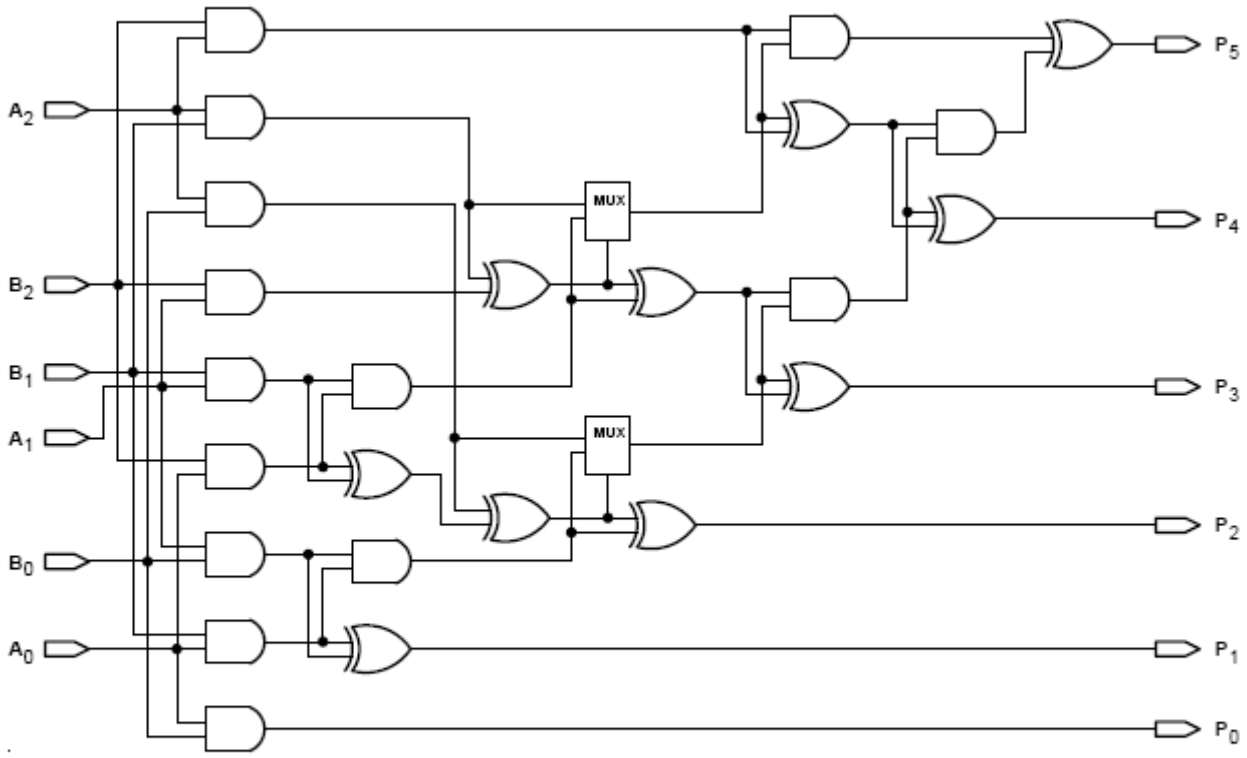


Figure 16: Most efficient conventional three-bit multiplier (30 two-input gates, 26 gates with `MUX`).

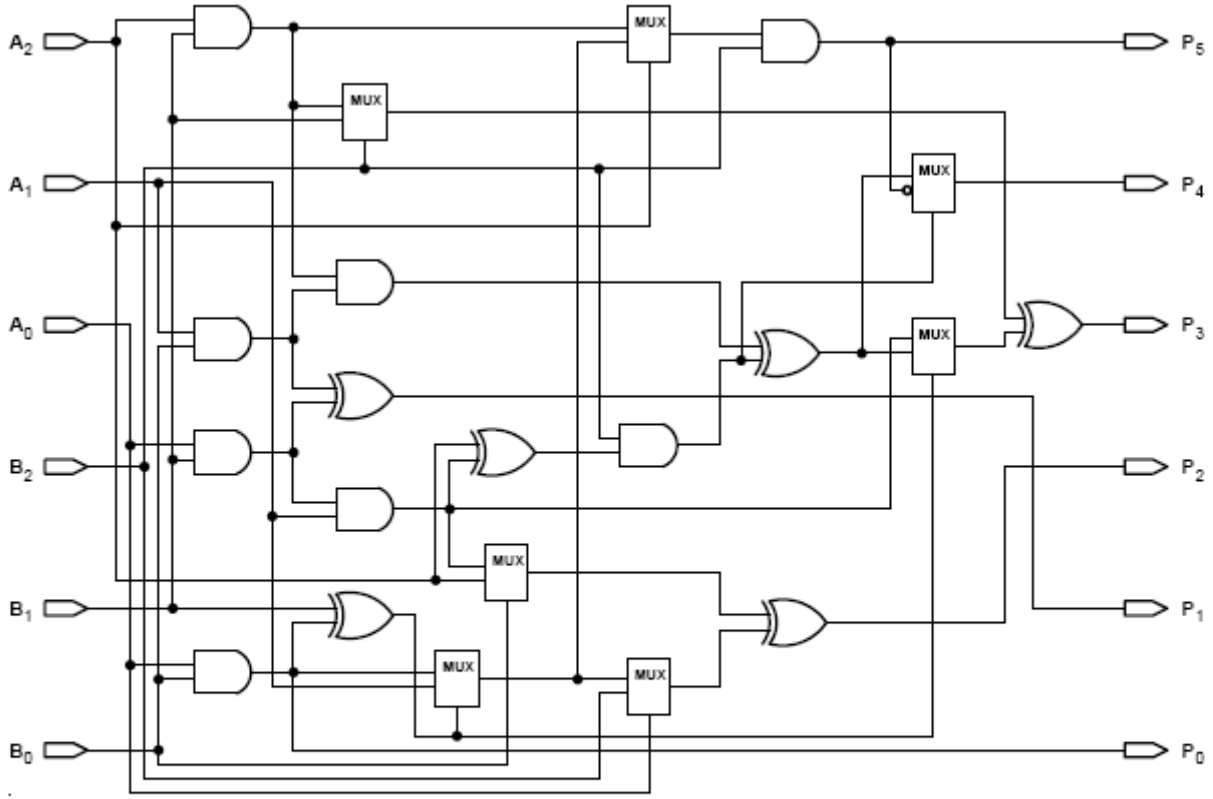


Figure 18: Evolved three-bit multiplier (21 gates = 14 two-input gates + 7 `MUX`).

Analog Design

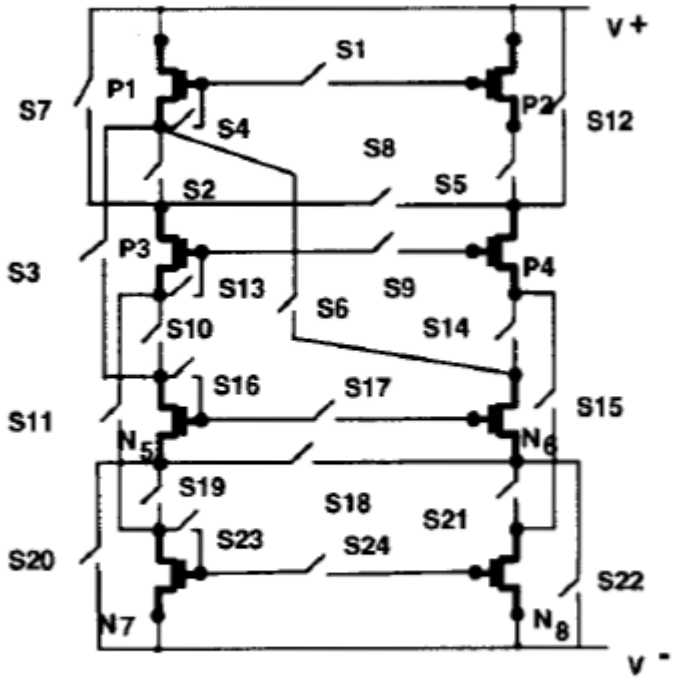


Figure 5. Module of the Field Programmable Transistor Array

(Stoica et al, 2000)

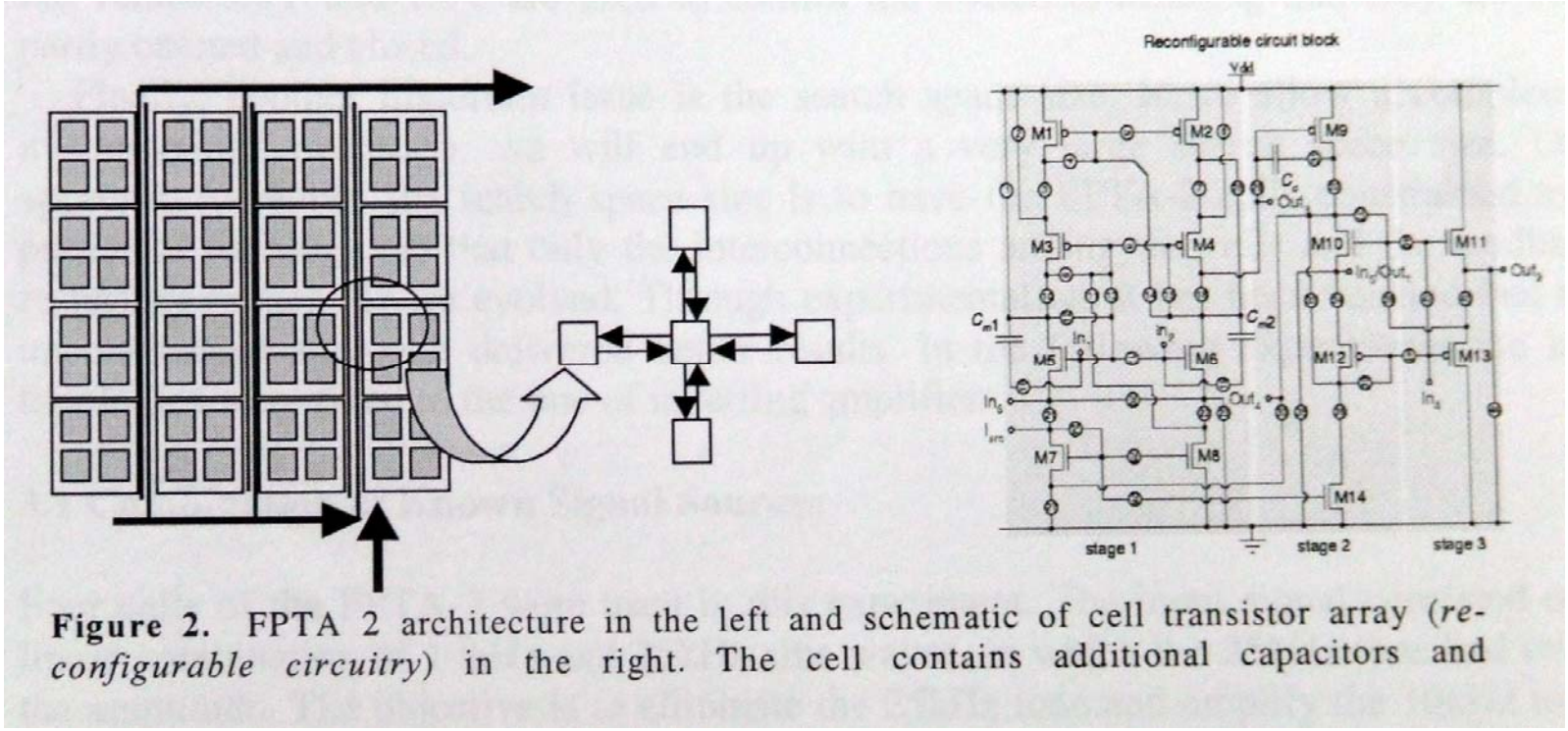


Figure 2. FPTA 2 architecture in the left and schematic of cell transistor array (*reconfigurable circuitry*) in the right. The cell contains additional capacitors and

(Zebulum, 2003)

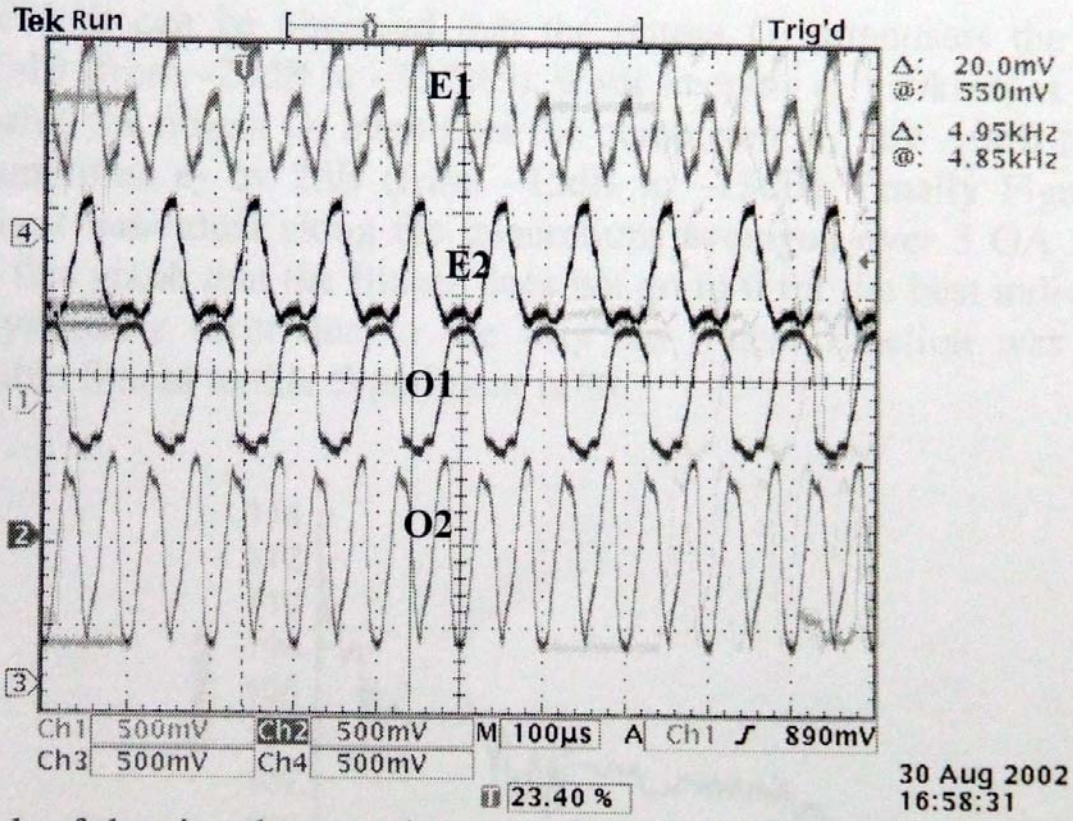


Figure 8: Result of the signal separation experiment. At the top the inputs E1 and E2 shown. At the bottom the outputs O1 (10kHz)) and O2 (20kHz) are shown.

(Zebulum, 2003)

Evolutionary Algorithms in Hardware

Compact Genetic Algorithm

(Harik, Lobo & Goldberg 1999)

1. Initialize probability vector

```
for i := 1 to L do p[i] := 0.5;
```

2. Generate two individuals from the vector

```
a := generate(p);
b := generate(p);
```

3 Let them compete

```
Winner, loser := evaluate(a, b);
```

4. Update the probability vector toward the better one

```
for i := 1 to L do
 if winner[i]  != loser[i] then
    if winner[i] = 1 then p[i] += 1/N
    else p[i] -= 1/N
```

5. Check if the probability vector has converged

```
for i := 1 to L do
 if p[i] > 0 and p[i] < 1 then goto step 2
```

6. P represents the final solution

Fig. 1. Psedocode of Compact Genetic Algorithm

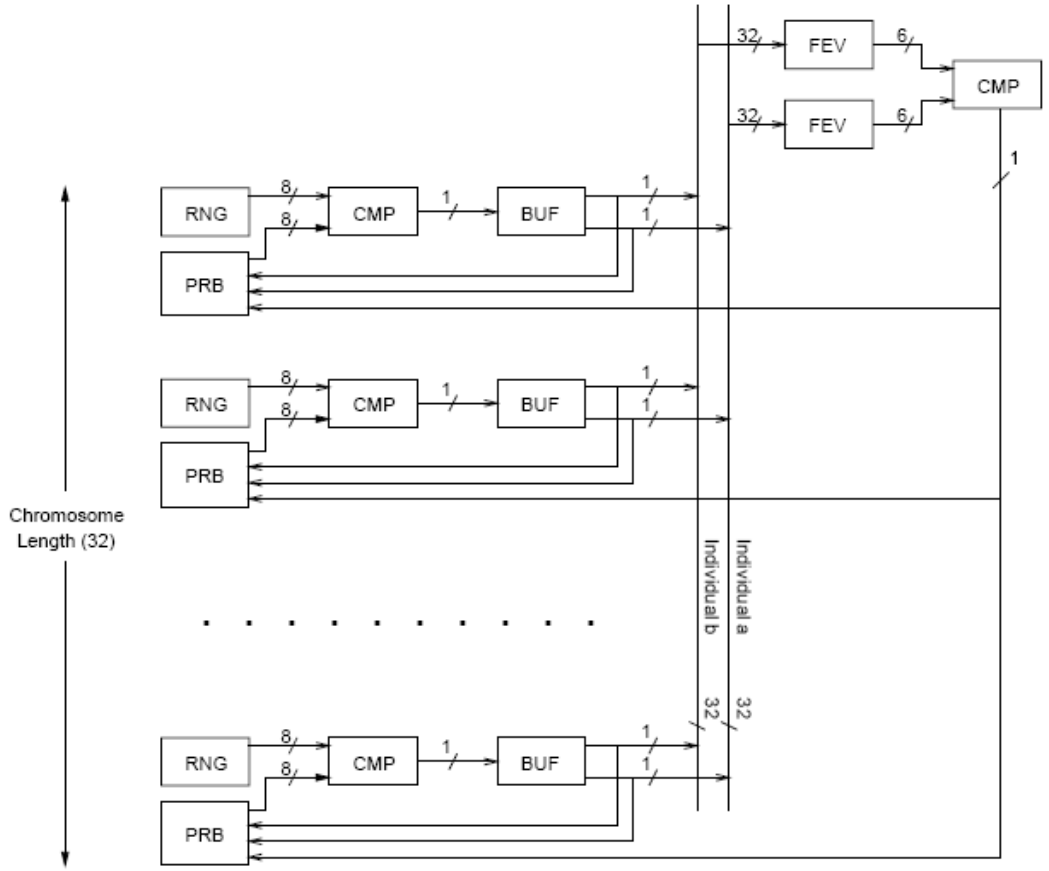
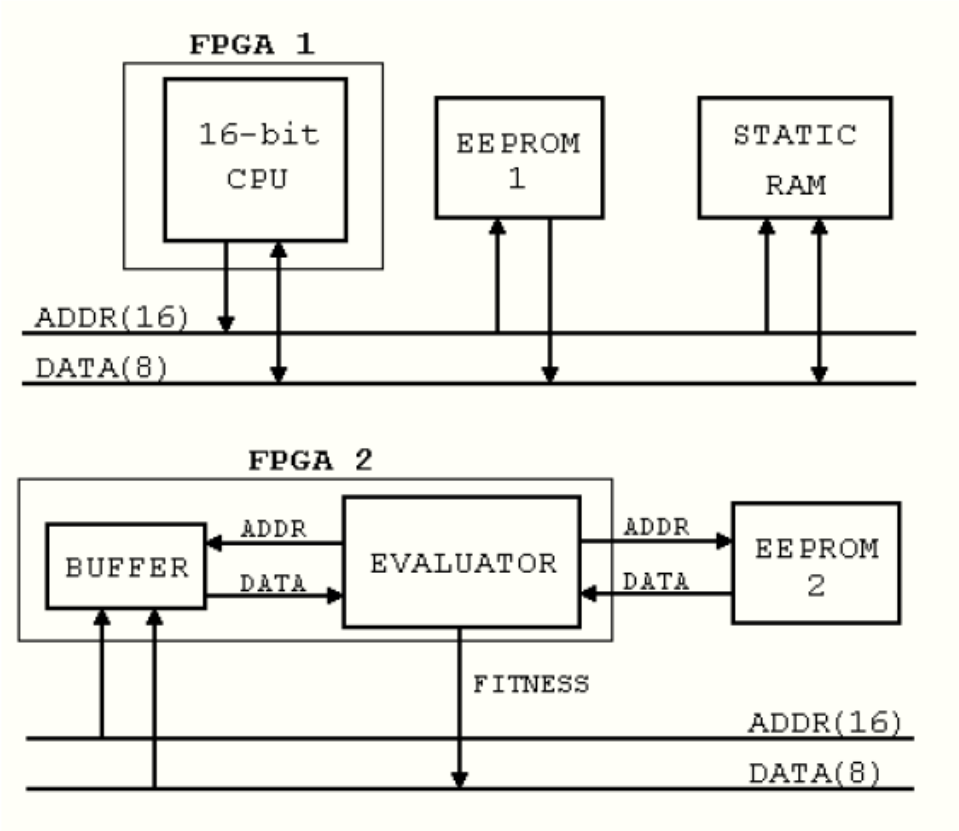


Figure 2: Hardware organization (population size = 256, chromosome length = 32).

(Aportewan & Chongstitvatana 2001)



(Aportewan & Chongstitvatana, 2000)

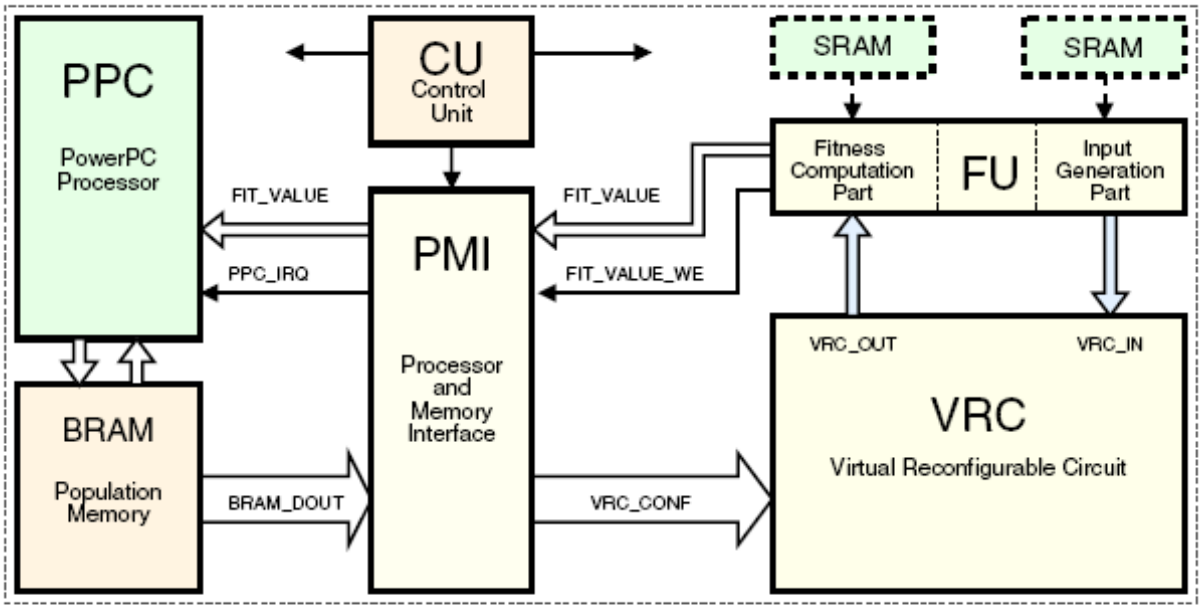


Fig. 3. Generic architecture of CGP accelerators in the FPGA Virtex 2 Pro

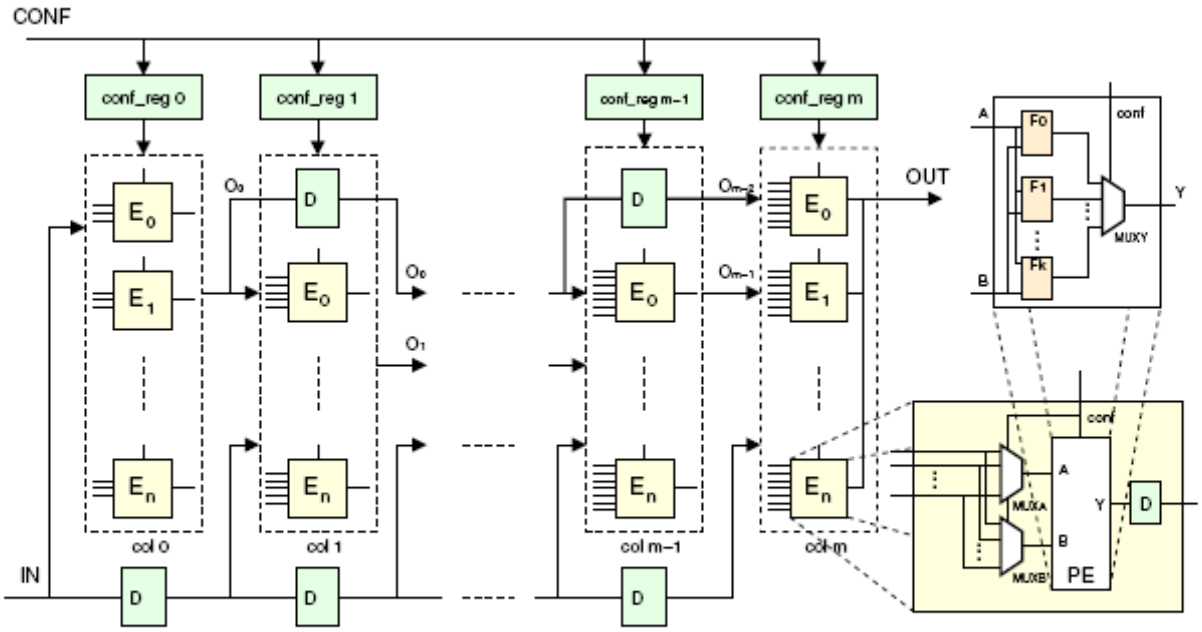


Fig. 5. VRC for evolution of digital circuits

(Vasicek, Z. and Sekanina, L., 2008)

Scalable Compact Genetic Algorithm in Hardware

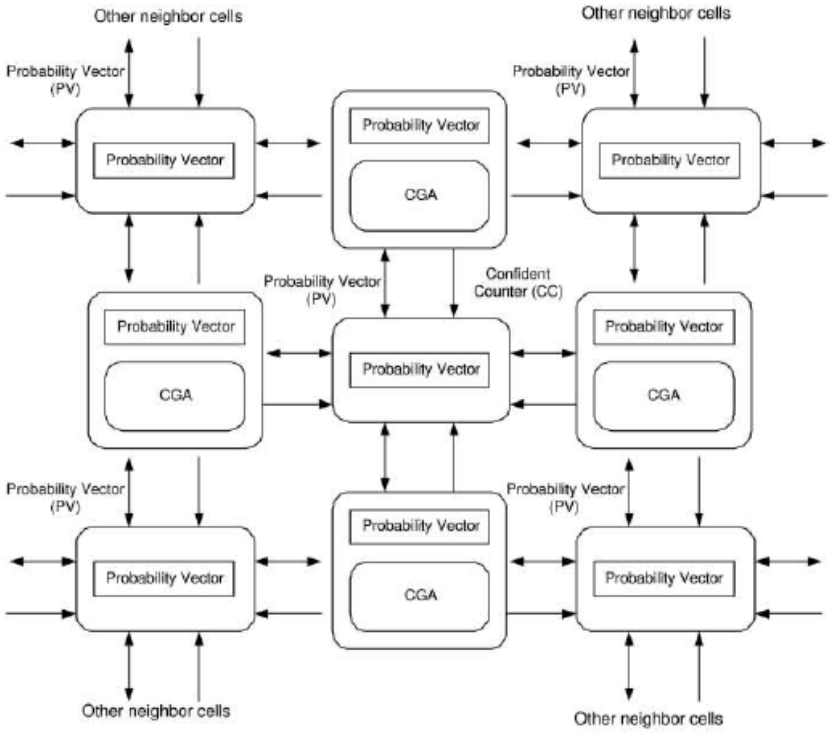


Fig. 2. Cellular Automata (CA)-like topology for Cooperative Compact GA

(Jewajinda, Y. and Chongstitvatana, P., 2006)

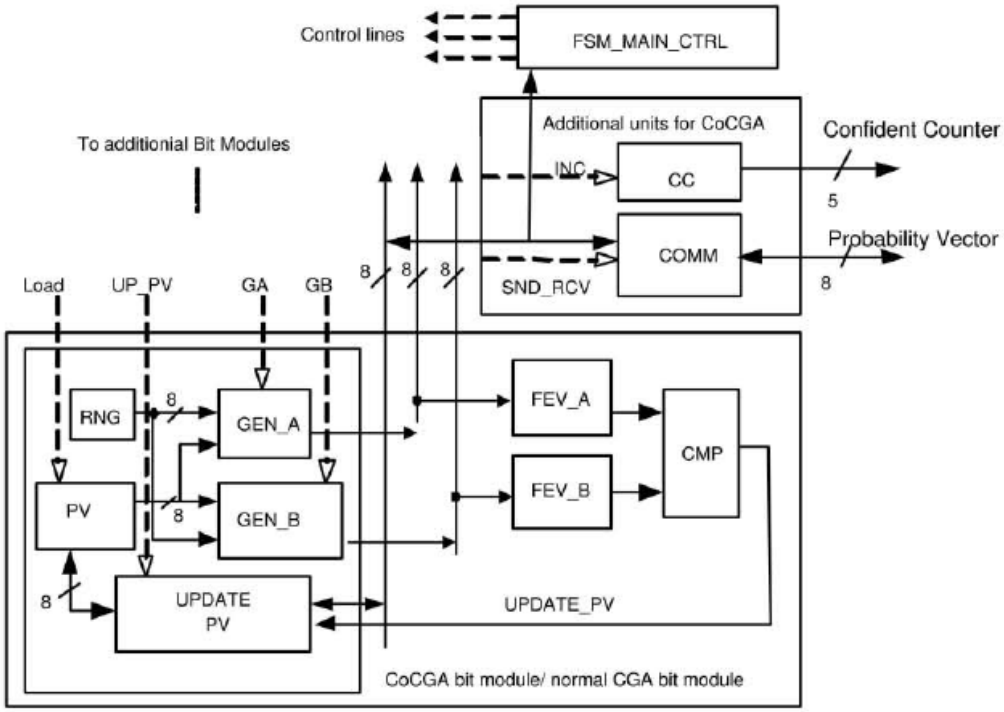


Fig. 5. Hardware block diagram of CoCGA cell

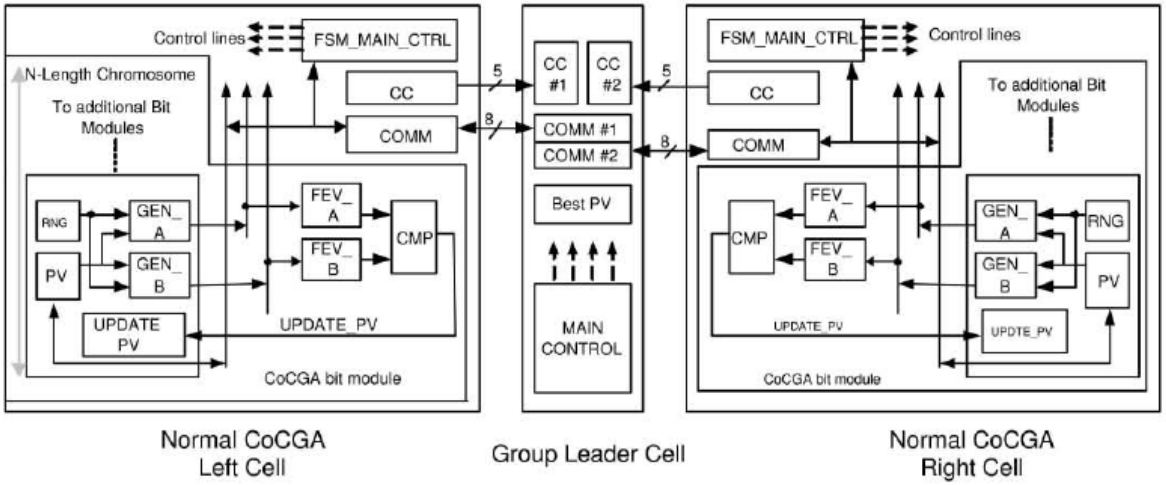
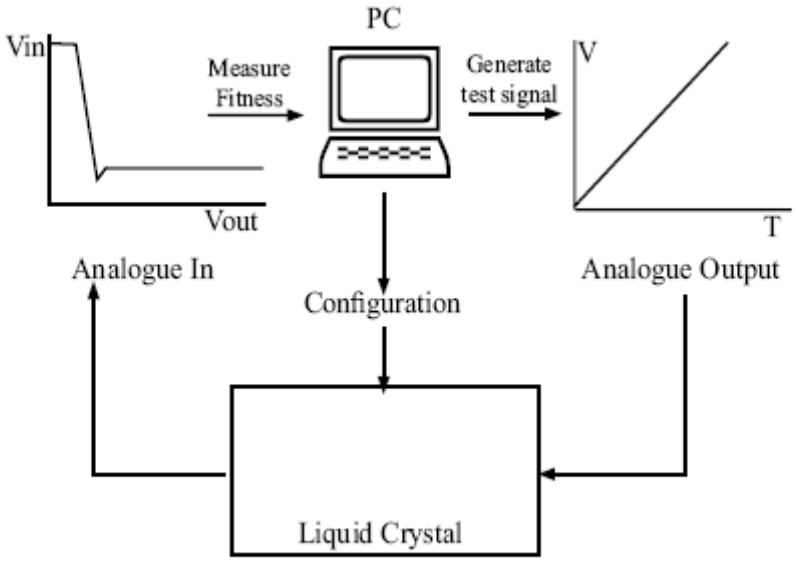


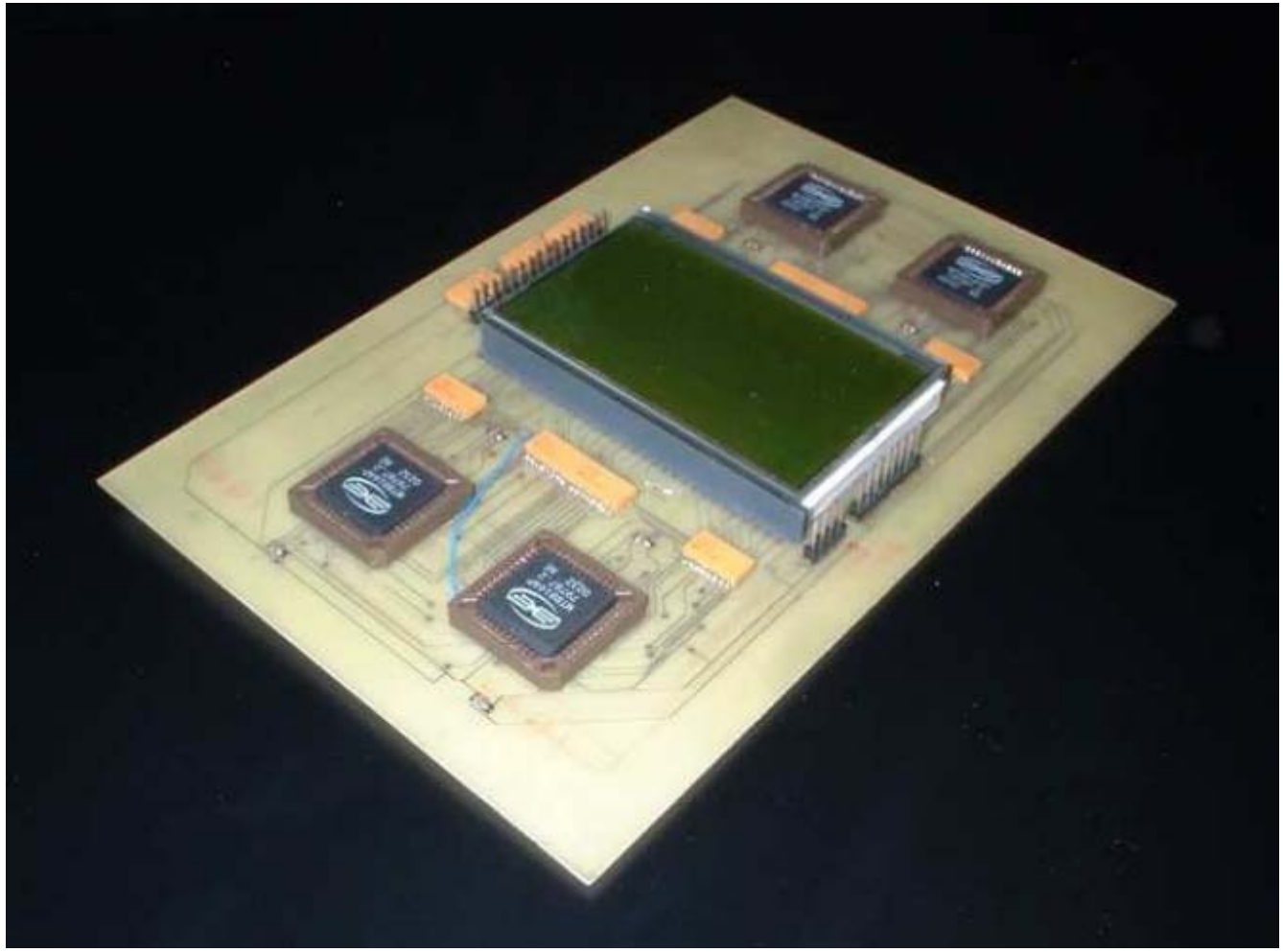
Fig. 6. Hardware block diagram of CoCGA with two neighbors

Other Curiosities

Liquid Crystal as a medium

(Hardy & Miller, 2004)





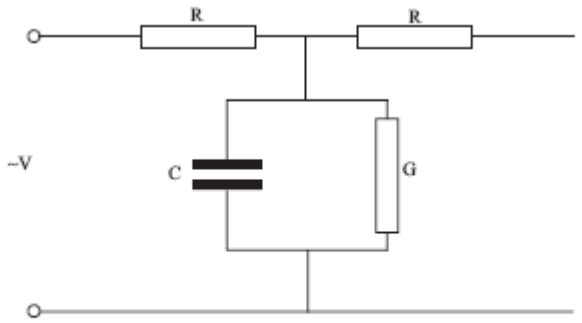
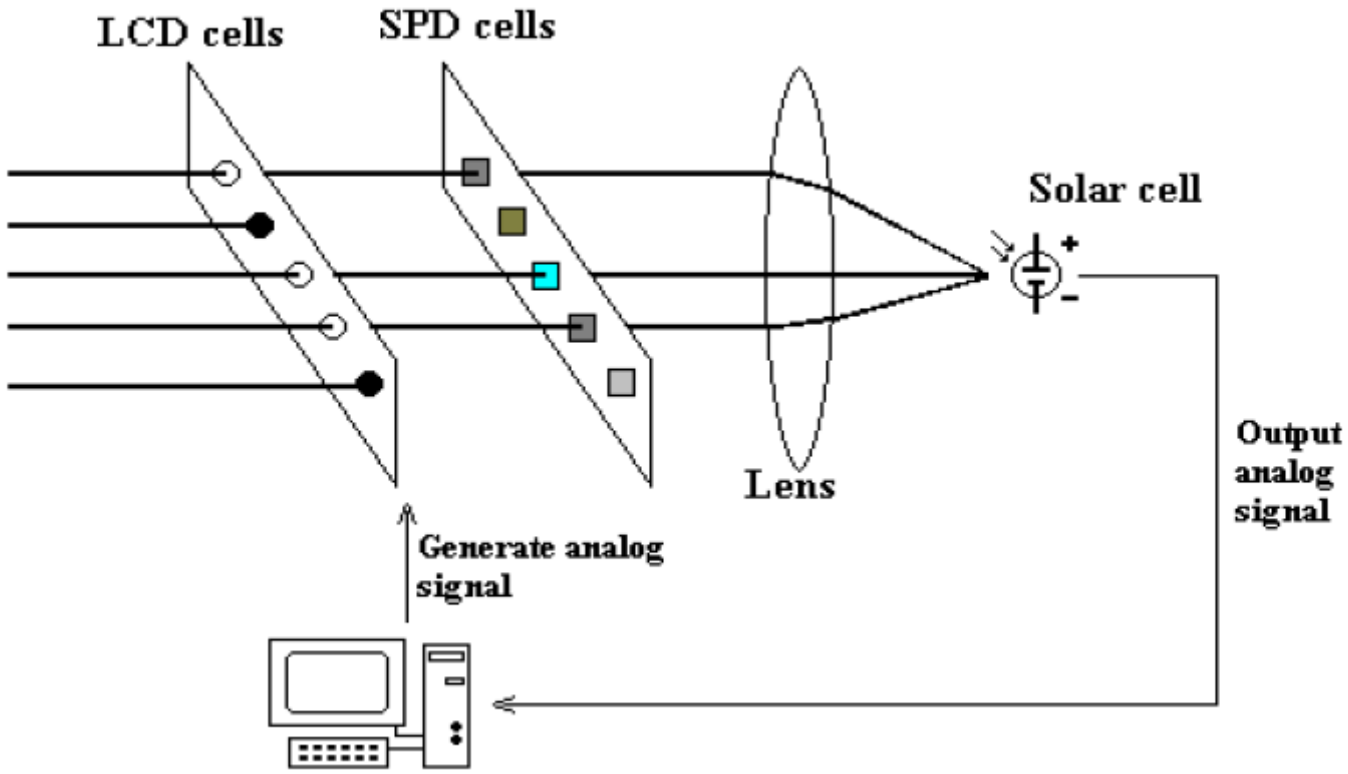


Figure 1. Equivalent circuit for LC

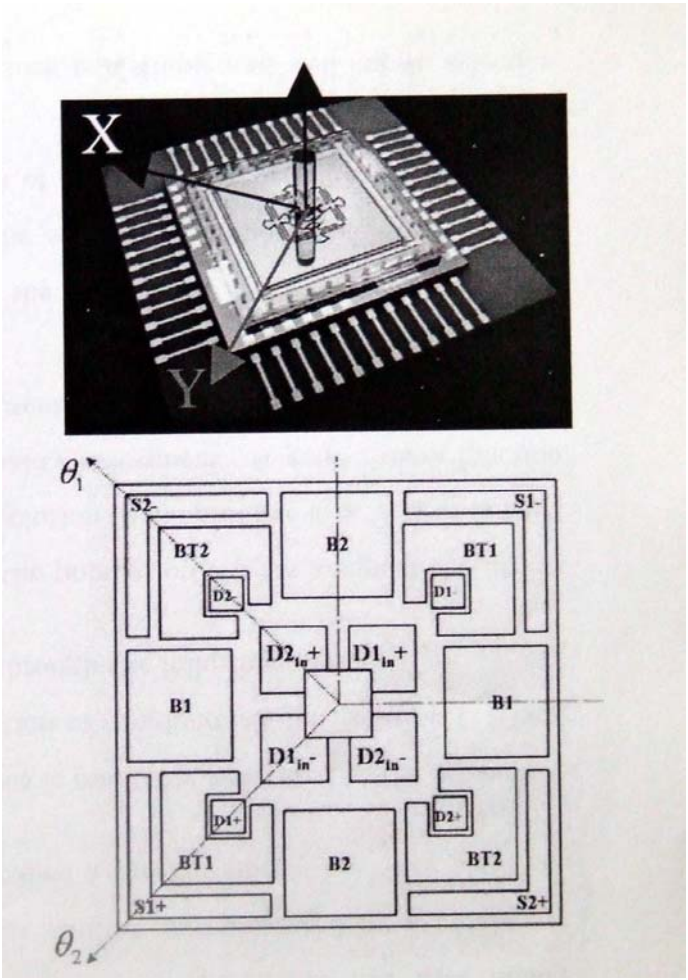

LCD cells
SPD cells
Lens
Solar cell
+
-
Output analog signal
Generate analog signal

(Oltean, 2006)

Tuning MEMS gyroscope

(Ferguson et al, 2005)

Tuning the resonance frequencies to be symmetric.
The tuning pads are electrostatically soften the mechanical springs.


X
Y
θ_1
S2-
S1-
BT2
B2
BT1
D2-
D1-
$D2_{in}$+
$D1_{in}$+
B1
B1
$D1_{in}$-
$D2_{in}$-
D1+
D2+
BT1
B2
BT2
S1+
S2+
θ_2

Cooperative GA in hardware + Neural Network

(Jewajinda & Chongstitvatana, 2008)

Block-based Neural Network

(Moon & Kong, 2001)

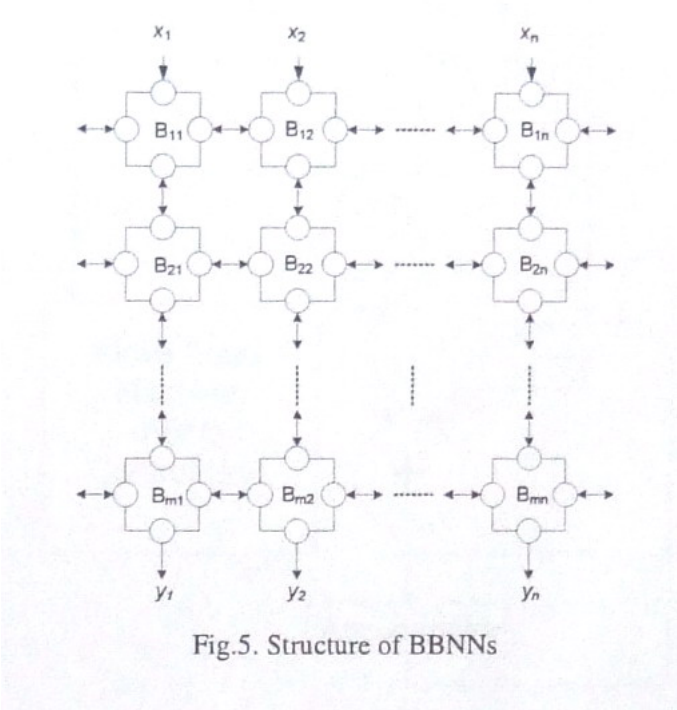


Fig.5. Structure of BBNNs

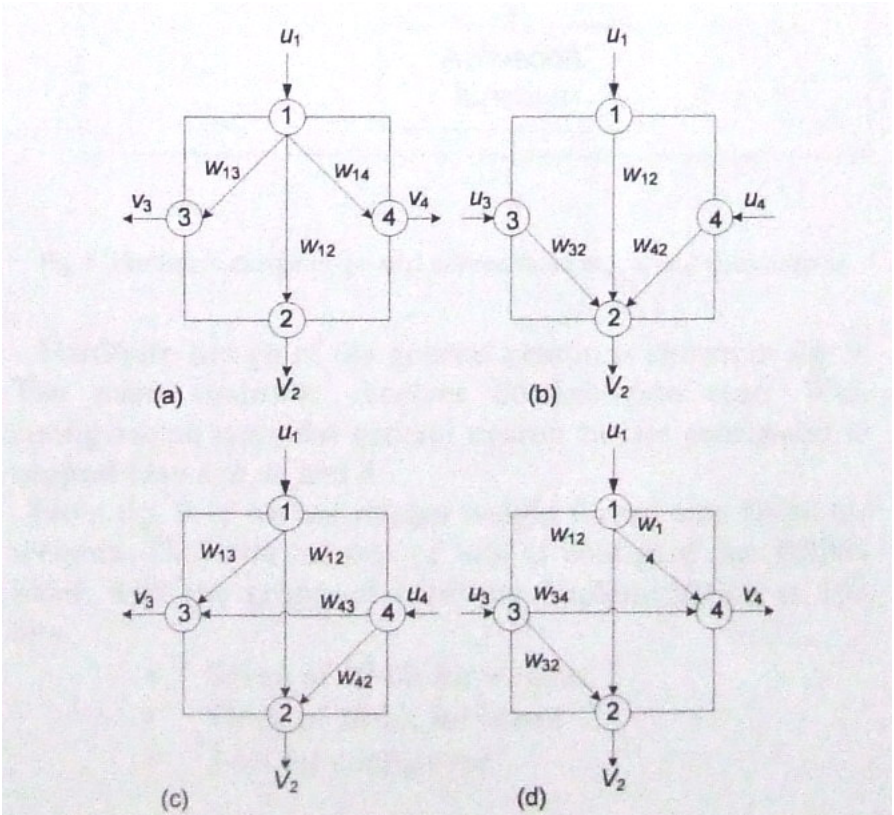


Fig.6. Four different internal configurations of a BBNN block (a) 1/3, (b) 3/1, (c) 2/2, (d) 2/2

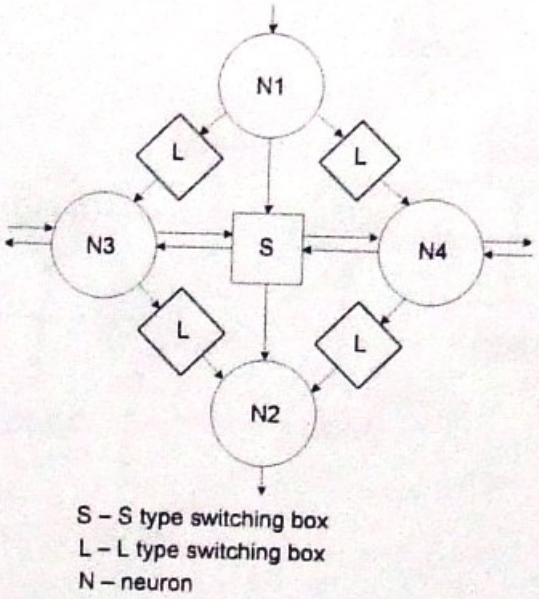


Fig.7. a BBNN block

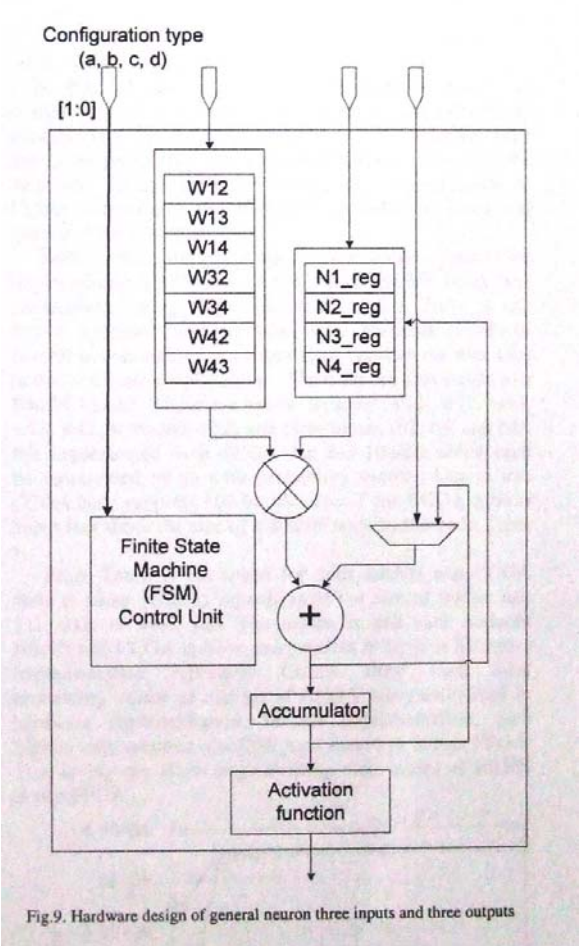


Fig.9. Hardware design of general neuron three inputs and three outputs

(Jewajinda & Chongstitvatana, 2008)

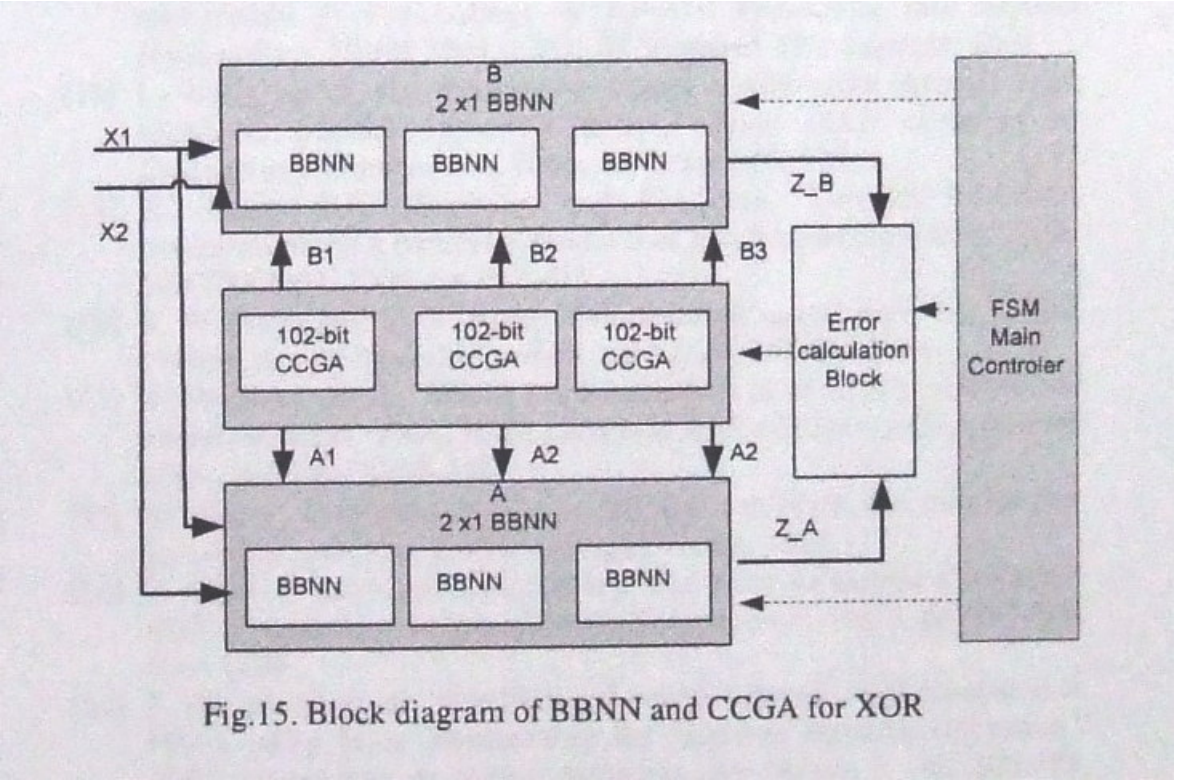


Fig.15. Block diagram of BBNN and CCGA for XOR

(Jewajinda & Chongstitvatana, 2008)

Current and Future Research

Applications

International Conf. on Evolvable System (ICES) 2007

Sonar spectrum classification
Fault tolerant analog circuits
Self repairing circuits
Underwater acoustic wireless communication
Adaptive air-to-air missile controller
Automatic adjustment for optical axes in laser systems
Analog circuits for space applications
Lossless image compression

Adaptive Hardware and System (AHS) 2006

Self-tuning analog PID controller
Temperature-adaptive circuits on analog arrays
Adaptive micro antenna
Drive control loop of gyroscope
H.624 adaptive deblocking filters
Low complexity self-calibrating adaptive quadrature receiver
Adaptable multiplier for cryptographic applications

Thank you