Development of a data reading device for a CD-ROM drive with FPGA technology

P. Nanthanavoot and P. Chongstitvatana
Department of Computer Engineering, Faculty of Engineering,
Chulalongkorn University, Bangkok 10330, Thailand.
Phone (66-2) 2218-6956, Fax 0-2218-6955 E-mail: prabhas@chula.ac.th

ABSTRACT

This paper presents a design of a device that can access a CD-ROM drive in the IDE standard. The device is implemented with Verilog HDL (Hardware Description Language) and FPGA (Field Programmable Gate Array) technology. The system consists of three components: (i) *Processing Unit* that controls all system operations, (ii) *Address Decoder* for managing the address space of data, stack and input/output ports and (iii) *IDE Host Adapter* for interfacing with a CD-ROM drive. The development begins with designing and coding the system in Verilog HDL. The simulation is performed to test that it can access data from the CD-ROM drive. Finally, the system is synthesized targeting a FPGA chip and the amount of resources is reported.

KEYWORDS: CD-ROM, IDE interface, ATA/ATAPI, Verilog HDL, FPGA.

1. INTRODUCTION

Presently, the world has fully acknowledged the importance of information and the requirement for data storage has grown exponentially. One of the widely used media is CD-ROM due to its many advantages, for instance, its large capacity at a lower cost and its more compact size compared to other media. Moreover the CD-ROM can be used with many types of platforms.

For many systems, which interface to a IDE device [1,2,3,4], most developers use software-programmable microcontrollers for accessing the devices in the IDE standard. For example, [1,2,3] use PIC 16F877 – 20 MHz clock as the processor to drive an IDE connector directly from its ports. These devices are software driven. Although it is easy to develop and modify, it has a high overhead execution in each IDE device accessing operation.

To reduce the execution overhead, this research focuses on designing a system which has a special hardware for interfacing between the processing unit and a IDE CD-ROM drive. The system is implemented with FPGA (Field-Programmable Gate Array) technology. It is designed in RTL (Register-Transfer Level) model and coded in Verilog HDL [5]. Because of these reasons, all system's component can be modified easily and can be implemented in one chip.

2. CD-ROM DRIVE AND IDE INTERFACE

The IDE interface is used in secondary storage, e.g. a hard disk, a CD-ROM drive and a tape drive. The IDE interface has a protocol called *ATA/ATAPI* (AT Attachment/ ATA Packet Interface) [6,7,8,9]. This protocol declares the characteristics and commands to access IDE device. CD-ROM drive uses the commands, which are defined in ATAPI protocol.

To use a CD-ROM drive, such as requesting an identical information, reading raw data or resetting the drive, the access is through specific internal registers in the CD-ROM drive. Four signals to access these registers are: *CS[1:0]-*, *DA[2:0]*, *DIOR-* and *DIOW-*. The requested data is transferred by 16-bit data bus: *DD[15:0]*. The internal registers in a CD-ROM drive consist of two blocks: *Command Block Register* and *Control Block Register*, which are selected by *CS[1:0]-* signal. The *DA[2:0]* signal is used to choose a register in that block. Reading and writing registers may perform different functions. The details are defined in *ATA/ATAPI* protocol.

The timing constraint, timing diagram and minimum period of accessing registers, in PIO mode 4 (Programmable Input/Output) of ATA/ATAPI protocol are shown in Figure 1 and Table 1.

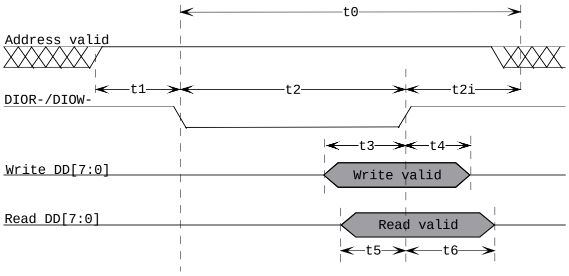

Figure 1. Timing diagram in accessing registers.

Register transfer timing parameters			Time
t_0	Cycle time	(min)	120 ns
t_1	Address valid to read/write setup	(min)	25 ns
t_2	DIOR-/DIOW pulse width	(min)	70 ns
t_{2i}	DIOR-/DIOW recovery time	(min)	25 ns
t_3	DIOW- data setup	(min)	20 ns
t_4	DIOW- data hold	(min)	10 ns
t_5	DIOR- data setup	(min)	20 ns
t_6	DIOR- data hold	(min)	5 ns

Table 1. Minimum period of accessing registers.

3. SYSTEM DESIGN

The system is designed in RTL (Register Transfer Level). It is synthesized and implemented with FPGA. The system is separated into 3 parts: Processing Unit, Address Decoder and IDE Host Adapter. The system block diagram is shown in Figure 5, which is at the end of this article.

3.1 PROCESSING UNIT

The processing unit in this system is developed for an embedded web server [10]. It is expected to replace the MCS-51 microcontroller in that work. The processing unit is a 16-bit processor, it has no pipeline and no interrupt. There are two 16-bit buses for data and instructions. The memory is divided into two parts: instruction memory and data memory. This processing unit has four 16-bit registers and two flags. A block diagram of the processing unit is shown in Figure 6.

The processing unit has twenty-seven 16-bit instructions. The instructions are divided into three groups: (i) Arithmetic and Logic instructions, (ii) Jump instructions and (iii) Load/Store instructions.

Because the processing unit is designed to be used in embedded systems, the architecture of the processing unit is simple and compact. The whole system is small enough to be implemented on a FPGA with spare resources for I/O interface.

3.2 ADDRESS DECODER AND ADDRESS SPACE MANAGEMENT

The processing unit has no specific I/O instructions. Memory-mapped I/O [11] is used to interface between the processing unit and I/O devices. The processing unit accesses I/O devices through Load/Store instructions for reading or writing data to I/O registers. The system address space is separated into three portions: (i) address FFF0-FFFF is assigned for I/O access, (ii) address FF00-FFEF is assigned for stack and (iii) address 0000-FEFF is data memory allocation. The address space is shown in Figure 2.

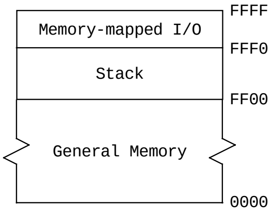

Figure 2. The address space definition.

The module, which manages the system address space, is Address Decoder. It decodes a data address of Load/Store instruction and sends the requested signals to data memory or I/O devices.

3.3 IDE HOST ADAPTER

The CD-ROM drive is accessed through its internal registers. The IDE Host Adapter is a special purpose hardware, its function is to handle accessing internal registers in the CD-ROM drive. The processing unit controls the IDE Host Adapter through 3 registers in the IDE Host Adapter. The adapter block diagram and its register are shown in Figure 3 and Table 2.

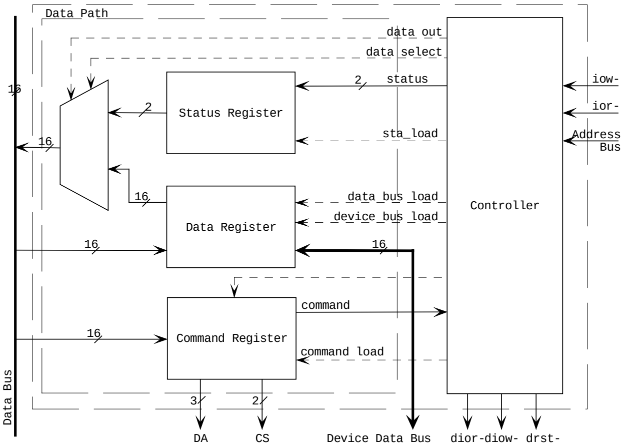

Figure 3. IDE Host Adapter block diagram.

Register Name	Address	Read/Write
Host Status	FF08	Read Only
Data Buffer	FF09	Read/Write
Command Buffer	FF0A	Write Only

Table 2. Registers in IDE Host Adapter.

- Host Status Register is a register, representing the status of the adapter. It is a 2-bit register. The first bit (bit 0) is a status of data that is kept in Data Buffer Register and the second bit (bit 1) is IDE Host Adapter working status.
- Data Buffer Register is a 16-bit register that stores data while reading or writing from/to internal registers in the drive.
- Command Buffer Register is a 6-bit register that stores a command, which specifies an address for accessing an internal register in the drive.

The IDE Host Adapter supports the CD-ROM drive in PIO mode 4 (Programmable Input/Output). The access method begins with the processing unit checking the status of the IDE Host Adapter by polling data from Host Status Register until it indicates that the adapter is not busy (BSY bit in Host Status = 0). When it is ready, the processing unit sends a Store instruction to write a command, which defines the register access parameter (Read/Write- access, *CS[1:0]-* and *DA[2:0]*), to Command Buffer Register in the adapter. If the command in Command Buffer Register is a read request, the IDE Host Adapter will request data. The processing unit must poll data from Host Status Register until it indicates that data is ready in Data Buffer Register and then the processing unit can read the data from Data Buffer Register using Load instruction. If the command is a write command, the processing unit must store a data, which is required to be transmitted, to Data Buffer Register. After the adapter received the data, it will request and send the data to an internal register in the drive.

4. System simulation and Synthesis

After designing and coding, the system is simulated to test its functionality. The simulation is running on an artificial environment that is similar to the system working in the real world. This environment is separated into hardware modules and the program. The hardware modules are such as CD-ROM drive, ROM and RAM. They are implemented with behavioral models, which describe their timing. The program has all basic functionality for interfacing with a CD-ROM drive such as accessing the internal registers in the drive.

Figure 4 is a part of simulation result. The task is to read data from internal registers at *CS[1:0]-* = 10 and *DA[2:0]* = 101. From Figure 4, there are three steps in reading data: (i) The processing unit writes a command 110101 to Command Buffer in IDE Host Adapter. (ii) when the IDE Host Adapter receives a command, it requests data by sending signal *CS[1:0]-* = 10 and *DA[2:0]-* = 101. (iii) The processing unit polls data status until Host Status register is set to indicate the data is ready to be read, then the processing unit reads that data and keeps it in its general register.

Finally, the system is synthesized with Xilinx Foundation 2.1i Series tool, the synthesized result is shown in Table 3.

From the synthesized result in Table 3, the total resource is 3614 equivalent gates. It must be realized with a FPGA that has enough resource such as SPARTAN S20VQ100.

```
CPU Synthesis.
==============
Design Summary:
   Number of errors:        0
   Number of warnings:      1
   Number of CLBs:            170 out of   400   42%
      CLB Flip Flops:      19
      4 input LUTs:       292
      3 input LUTs:        45
   Number of bonded IOBs:      69 out of    77   89%
      IOB Flops:           16
      IOB Latches:          0
   Number of clock IOB pads:    1 out of     8   12%
   Number of primary CLKs:      1 out of     4   25%
   Number of secondary CLKs:    3 out of     4   75%
Total equivalent gate count for design: 2486
Additional JTAG gate count for IOBs:    3312


Addressing Decoder.
===================
Design Summary:
   Number of errors:        0
   Number of warnings:      1
   Number of CLBs:              7 out of   400    1%
      CLB Flip Flops:       0
      4 input LUTs:        14
      3 input LUTs:         0
   Number of bonded IOBs:      18 out of    77   23%
      IOB Flops:            0
      IOB Latches:          0
Total equivalent gate count for design: 84
Additional JTAG gate count for IOBs:    864


IDE Host Adapter.
=================
Design Summary:
   Number of errors:        0
   Number of warnings:      1
   Number of CLBs:             58 out of   400   14%
      CLB Flip Flops:      39
      4 input LUTs:       105
      3 input LUTs:        10
   Number of bonded IOBs:      46 out of    77   59%
      IOB Flops:            5
      IOB Latches:          0
   Number of clock IOB pads:    1 out of     8   12%
   Number of primary CLKs:      1 out of     4   25%
   Number of secondary CLKs:    1 out of     4   25%
Total equivalent gate count for design: 1044
Additional JTAG gate count for IOBs:    2208
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Table 3. Synthesized result.

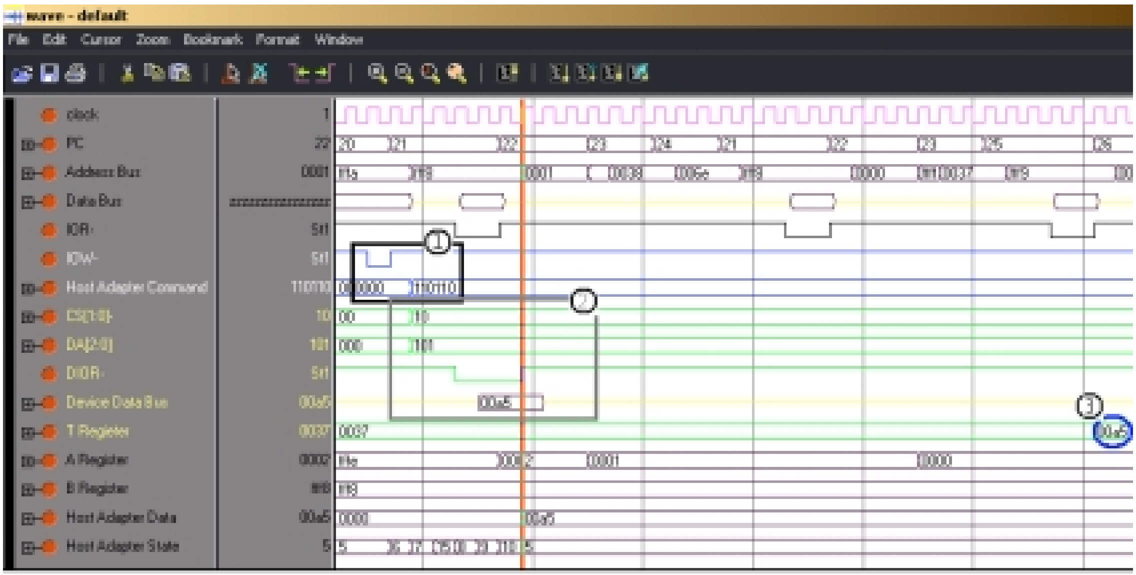

Figure 4. Simulation result.

5. CONCLUSION

This work presents a design and simulation of a system, which interface with a IDE CD-ROM drive. The advantage of using Verilog HDL in design is that the system can be modified easily. Because of FPGA technology, all system components can be synthesized into one chip.

The system has a special purpose hardware interface to the IDE CD-ROM drive so it has an advantage over the other design that use software-programmable microcontroller to access a CD-ROM drive directly. It reduce the execution overhead of microcontroller operations. Moreover it facilitates the development because programmers do not have to concern about timing constraints in the IDE standard.

6. REFERENCES

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ABOUT THE AUTHORS

Phanupan Nanthanavoot graduated in Bachelor degree of Computer Engineering, Chulalongkorn University, Thailand, 2001. He is studying Master degree of Computer Engineering, Chulalongkorn University, Thailand.

Prabhas Chongstitvatana earned BEng (EE) from Kasetsart University 1980 and PhD from the department of artificial intelligence, Edinburgh University, UK 1992. Presently, he is with the department of computer engineering, Chulalongkorn University. His research included robotics, evolutionary computation and computer architecture.

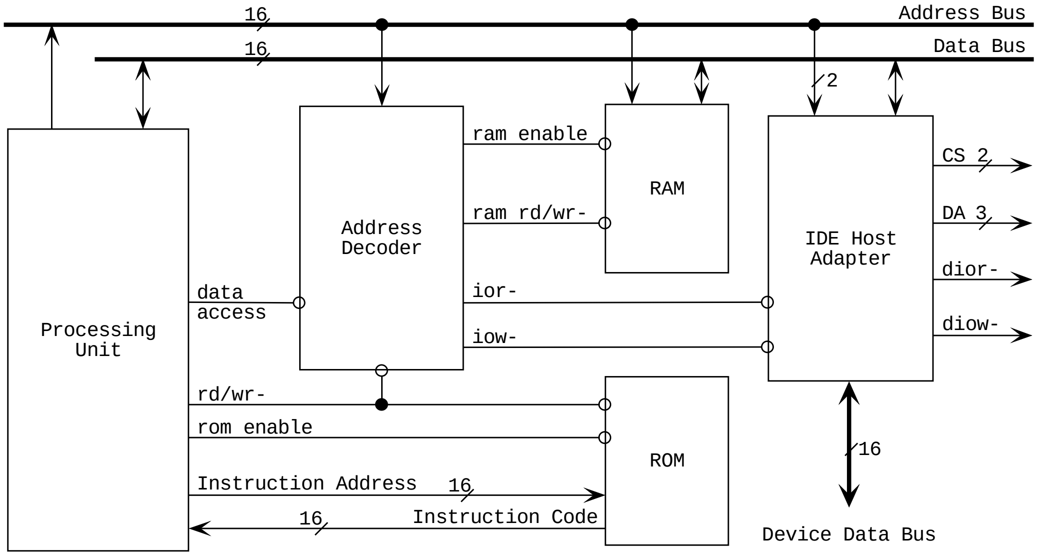

Figure 5. System block diagram.

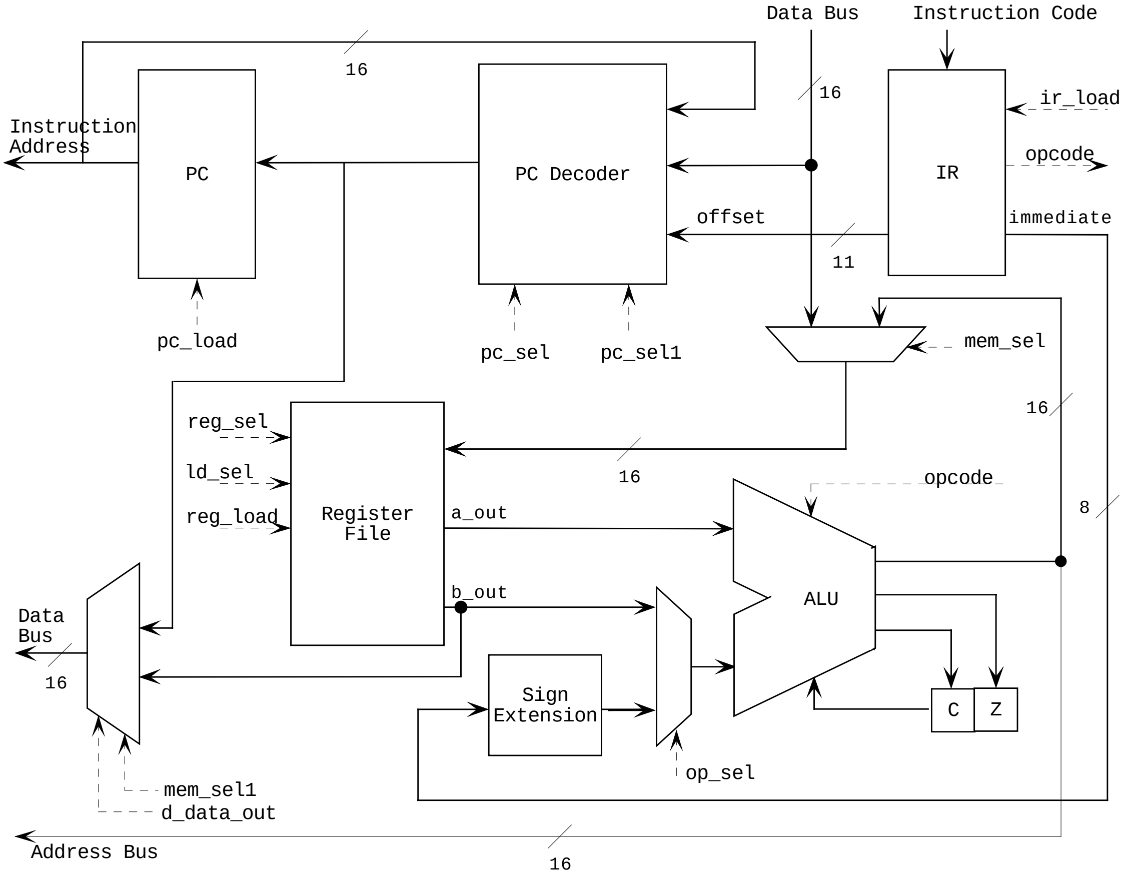

Figure 6. Processing Unit block diagram