Decrease Power Consumption using a Programmable Logic Device

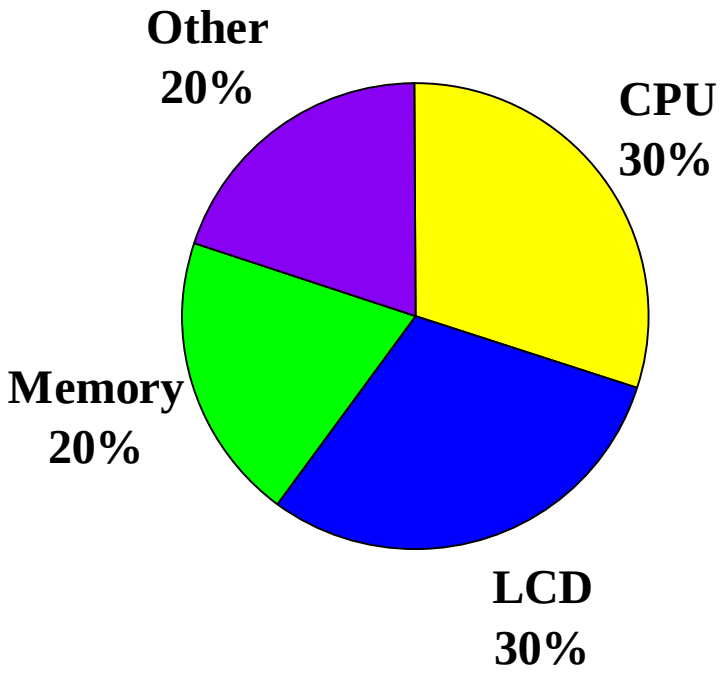
Jennifer Jenkins
Applications Engineer
Jennifer.Jenkins@xilinx.com

Introduction

- Existing power saving design techniques include:
  - Reducing operating voltage
  - Optimizing system and CPU clock frequency
  - Eliminating spikes of large current consumption during the power up sequence
  - Efficiently manage system battery operation
  - Efficiently managing operating mode of system devices
  - Minimizing bus activity
  - Reducing bus capacitance
  - Reducing switching noise
- Most important: managing operating mode of system devices
- What system devices?
  - Microprocessors
  - Microcontrollers

CPU Power Consumption

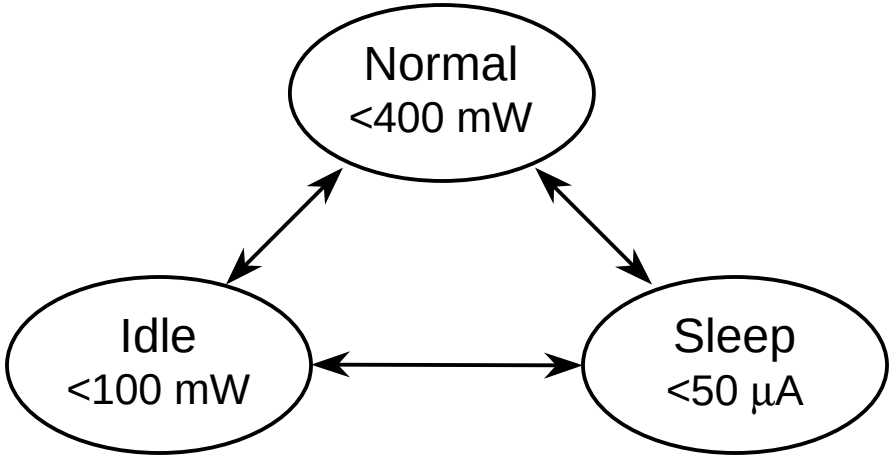
- Typical WebPad application*, CPU consumes 30% of overall power
- Range: 720uW to 1W during operation



* Data from International Data Corporation (IDC)

Operating Modes

- Microprocessor operating modes offer additional power savings to existing low power consumption
- Microprocessor puts itself in a low power mode when idle or suspended

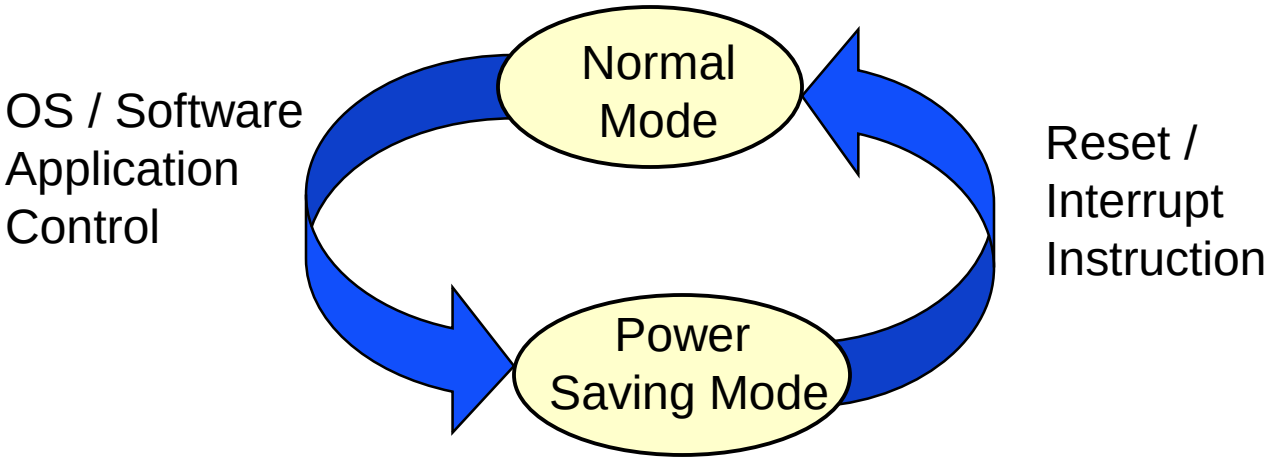


Intel® StrongARM SA-1110 microprocessor operating modes

(Power consumption shown is at 206MHz and V_{CCEXT}=3.3V and V_{CCINT}=1.8V)

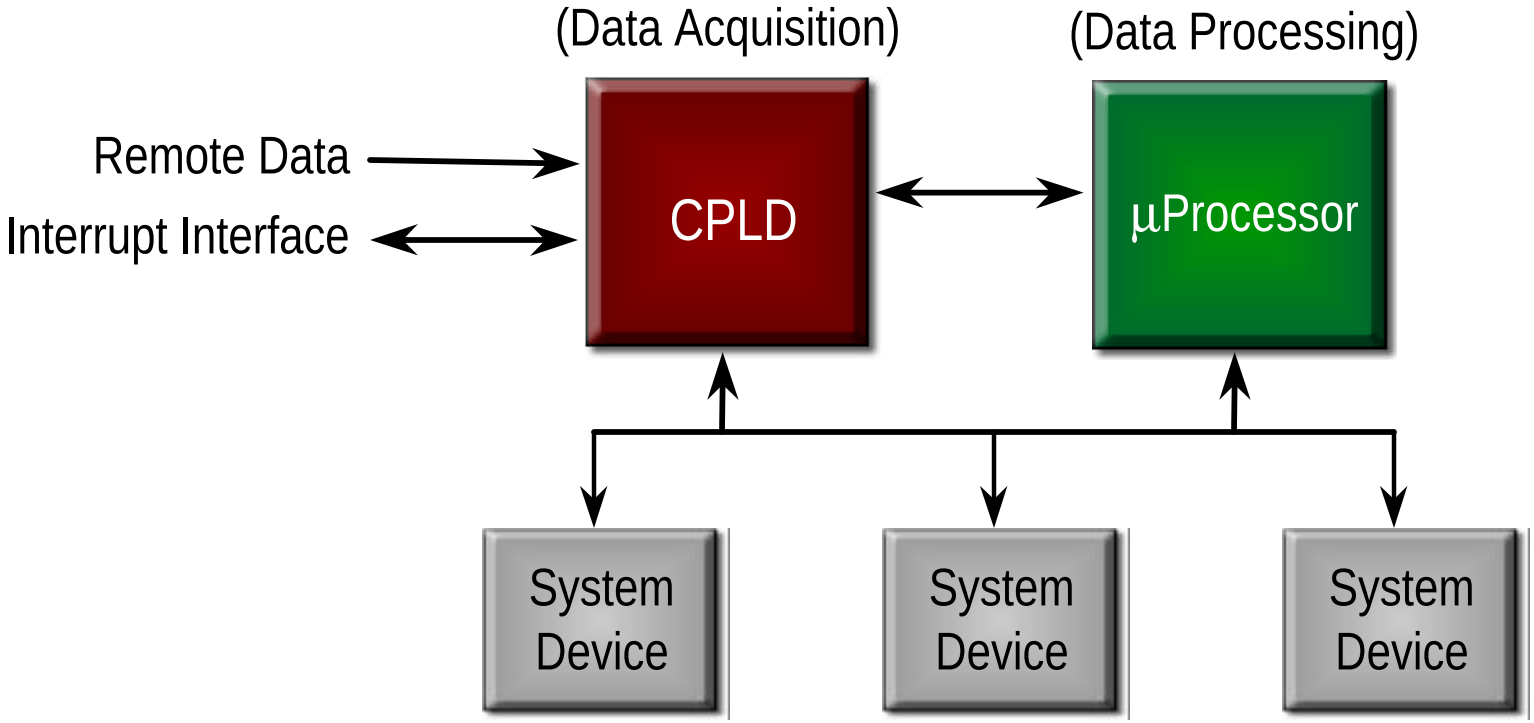
Operating Mode Control

- OS or software application temporarily suspend CPU
- Several operating modes allow further power savings
- Wake-up signals consist of HW reset, system interrupt, GPIO interrupt, OS timer interrupt, or peripheral interrupt



Using a CPLD

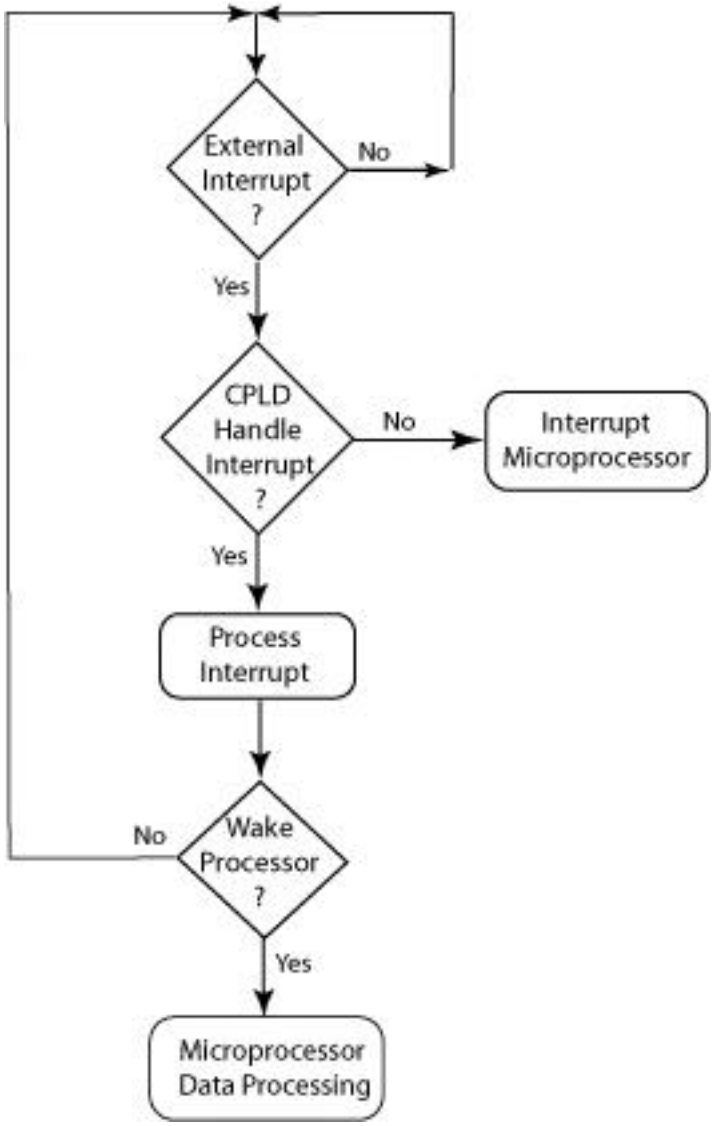
- Reduce number of interrupts to CPU
- Increase time CPU is in a power saving state
- Respond to and handle external CPU interrupts



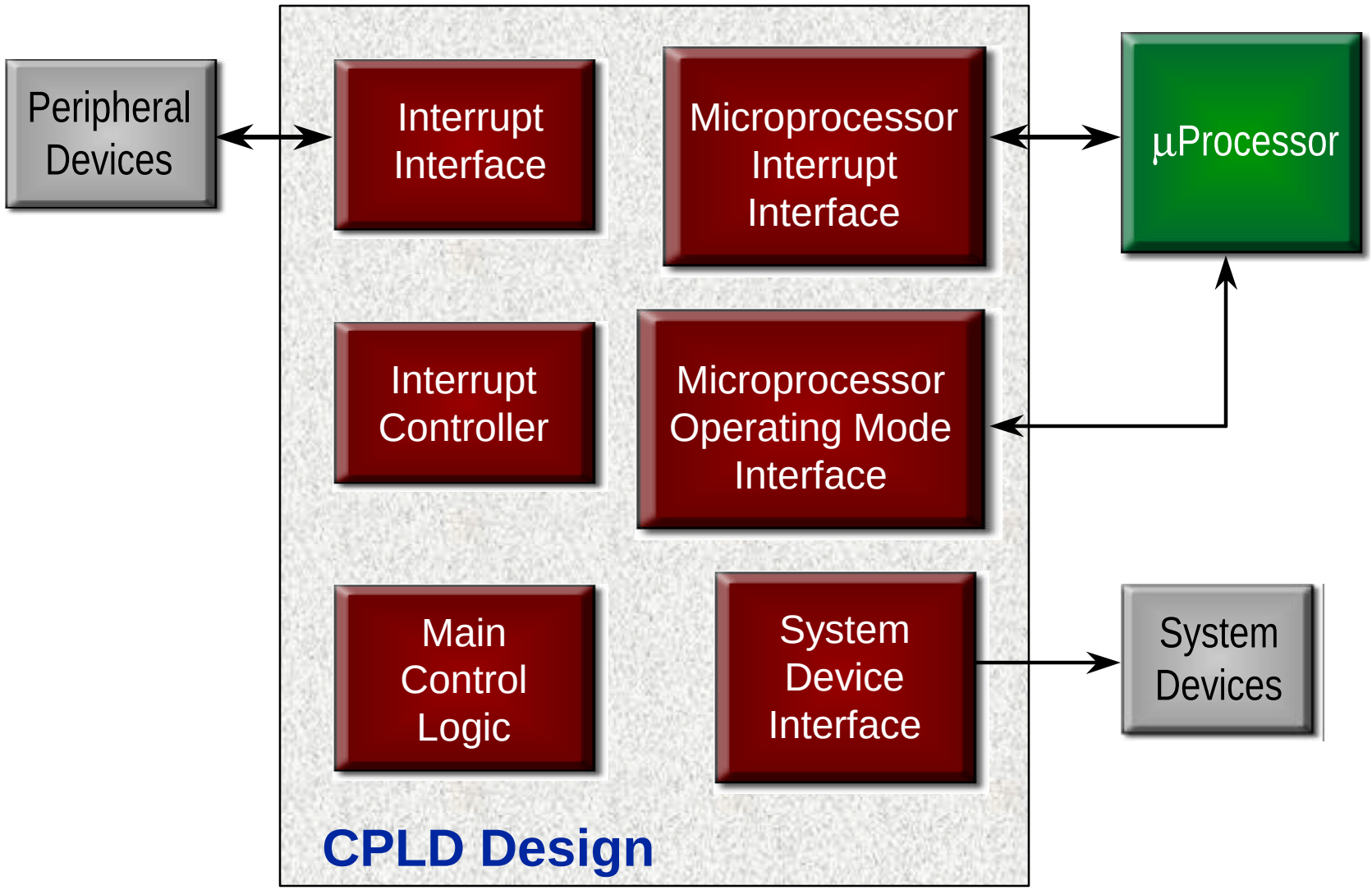
Function Separation

- Microprocessor = data processing operations
- CPLD = external interface, data acquisition operations
- System interrupts:
  - Memory access
  - Communication interfaces such as RF, I2C, UART, SPI, or ISA
  - General purpose I/O
  - LCD interface
- CPLD interrupt response time faster than microprocessor

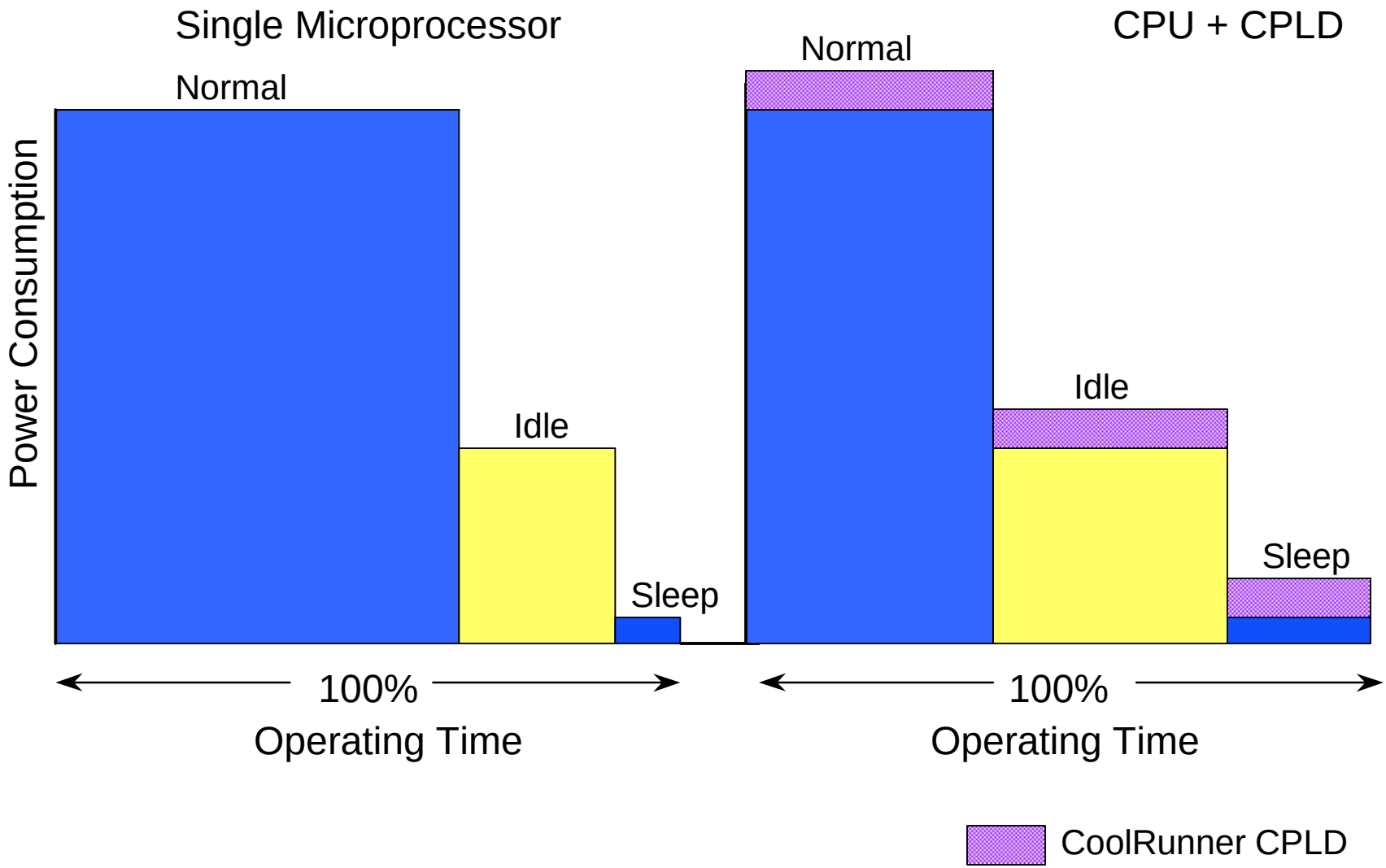
CPLD Operational Flow



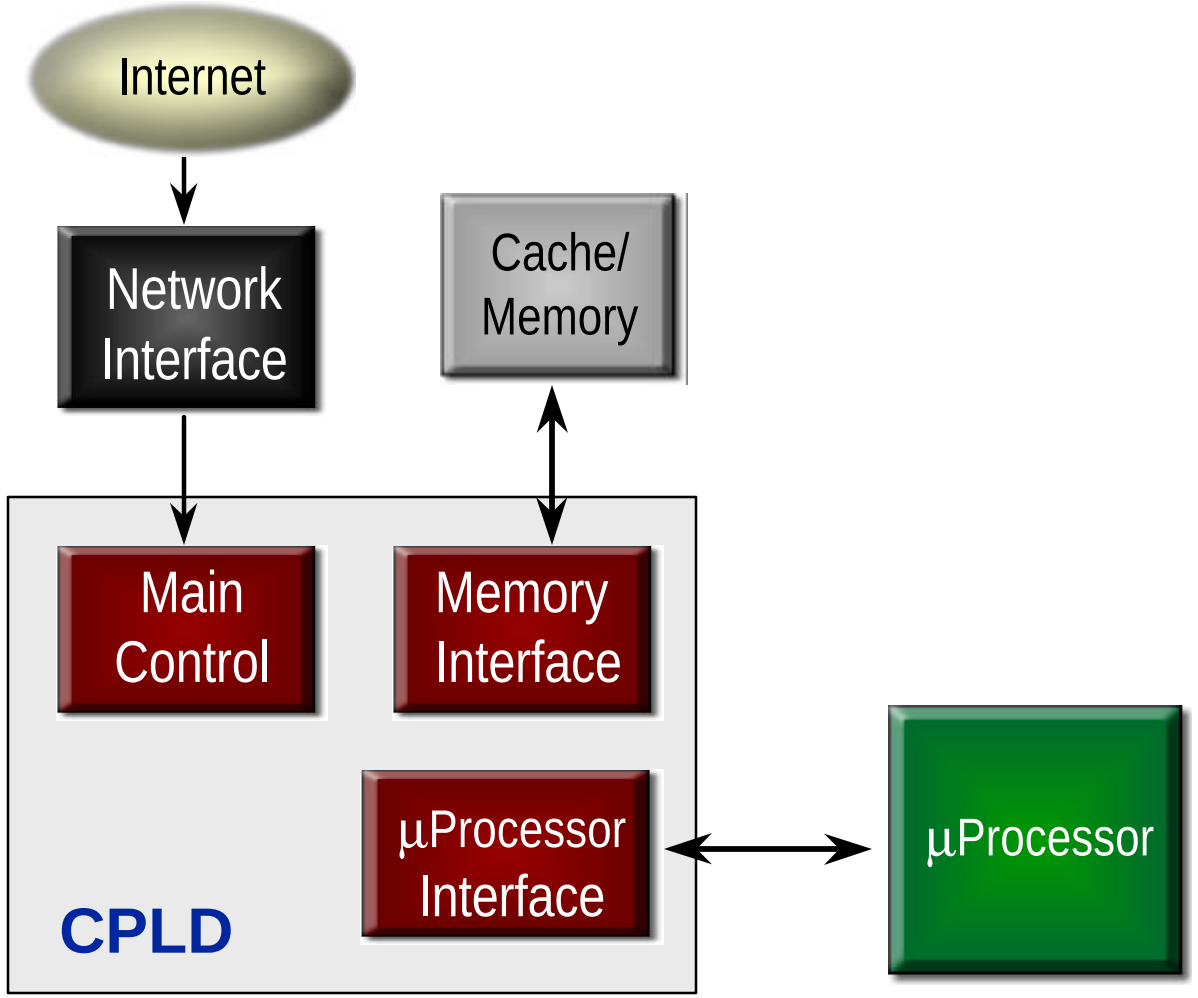
CPLD Functionality



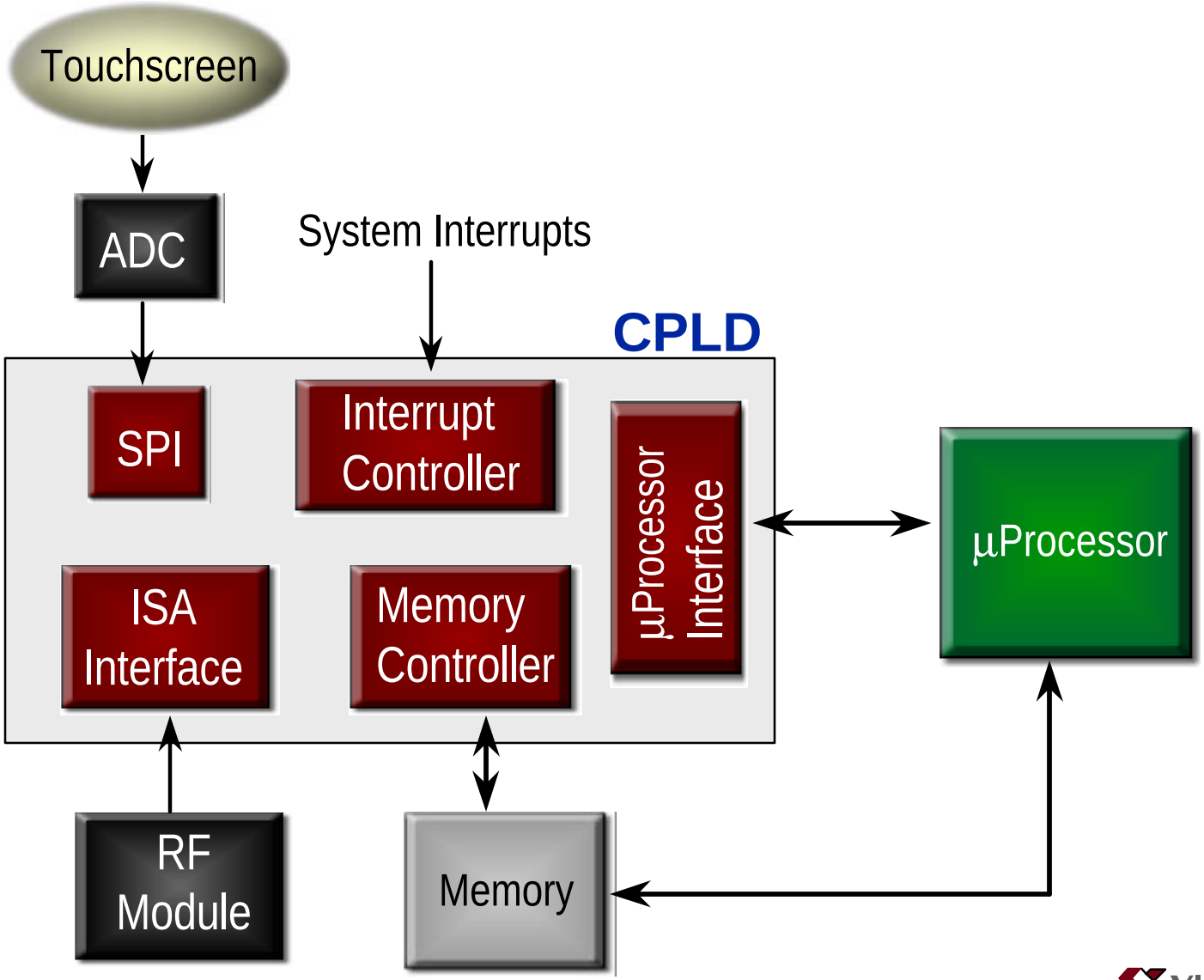
Power Savings



Email Terminal Example



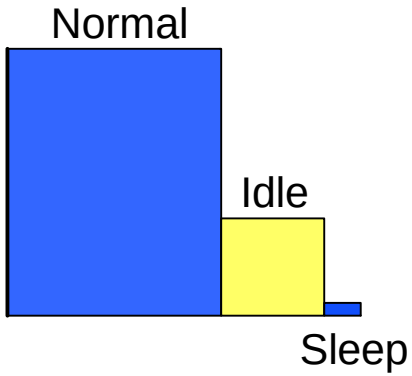
WebPad/PDA Example



CPLD Benefits

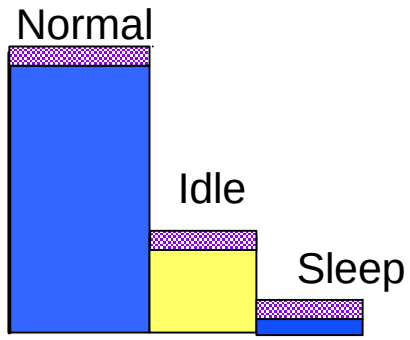
- Re-programmable CPLD provides flexible microprocessor interfacing
- Add additional system functionality:
  - Expand microprocessor I/O
  - Increase system interfaces
  - Smart battery management with SMBus interface
- Interface to multiple processors in multi-processor environment
- Xilinx CoolRunner CPLDs standby current < 100µA
- Operating power consumption of a CoolRunner CPLD fully populated with 16-bit counters and a 50MHz clock, I_{CC} is around 10mA

Power Savings



Single Processor Solution

Normal Mode	(60% of operating time)	= 24 Wh
Idle Mode	(30% of operating time)	= 3 Wh
Sleep Mode	(10% of operating time)	= 2.5 mWh
		27 Wh



Processor and CPLD Solution

Normal Mode	(40% of operating time)	= 16 Wh
Idle Mode	(30% of operating time)	= 3 Wh
Sleep Mode	(30% of operating time)	= 7.5 mWh
CPLD	(100% of operating time)	= 1.0 Wh
		20 Wh

Increase processor Idle and Sleep time equals additional power savings of **26%**

System Benefits Conclusion

- Increase processor time in sleep mode
- Faster response time to system interrupts
- Provide high speed interface to system with CPLD
- Run microprocessor at a lower frequency for data processing operations
- Increase performance of processor
- Extend battery life over product life cycle

Questions/Comments?

Email: Jennifer.Jenkins@xilinx.com

Web Address: www.xilinx.com