Evolvable Hardware

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An Overview of This Talk

This talk reviews the current work on EHW and points out some fundamental issues which remain open.

- What Is Evolvable Hardware (EHW)
- EHW as an Alternative to Electronic Circuit Design
- EHW as an Adaptive System
- Other EHW-Related Work
- Concluding Remarks

Evolutionary Techniques

On the Origin of Species (Darwin, 1859) :

evolution is based on "… one general law, leading to the advancement of all organic beings, namely, multiply, vary, let the strongest live and the weakest die."

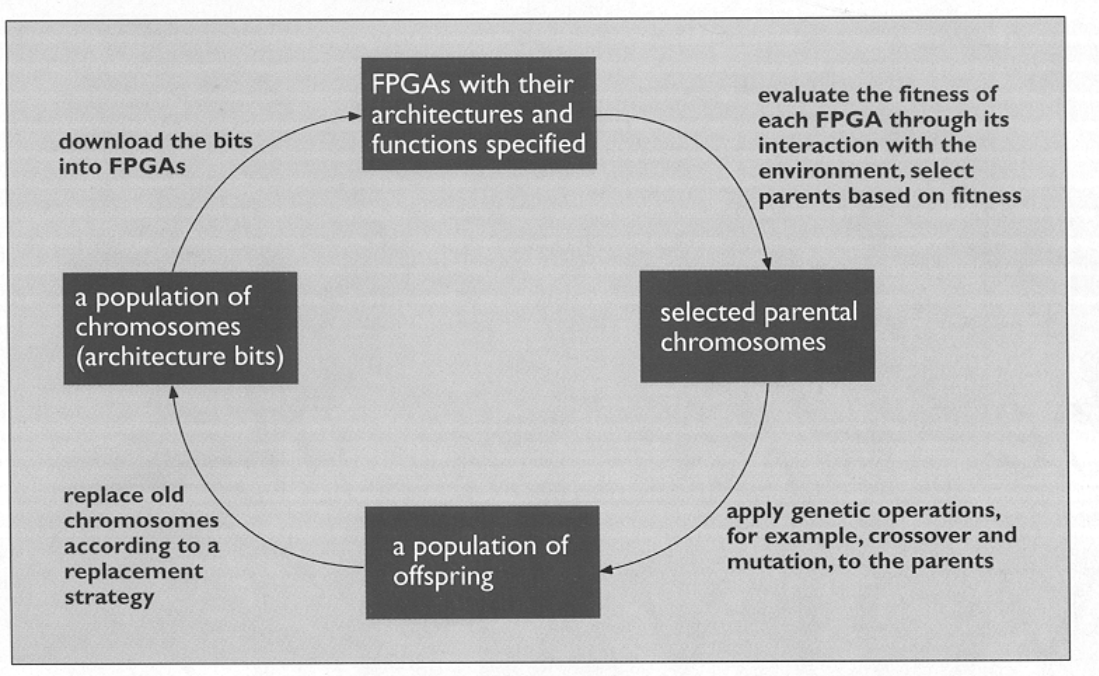
What Is Evolvable Hardware (EHW)

There are different views on what EHW is, depending on the purpose of EHW.

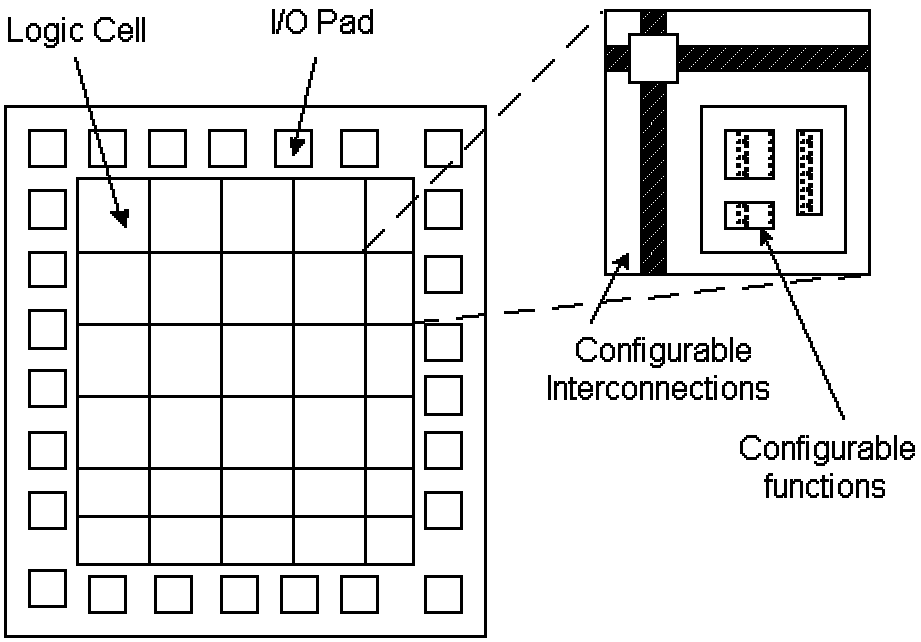
- EHW can be regarded as ``applications of evolutionary techniques to circuit synthesis." (A. Hirst)
- EHW is hardware which is capable of on-line adaptation through reconfiguring its architecture dynamically and autonomously. (T. Higuchi et al.)
- EHW refers to hardware that can change its architecture and behaviour dynamically and autonomously by interacting with its environment.

EHW How to

EHW is a child of the marriage between evolutionary computation techniques and electronic hardware.



Major steps in an evolutionary cycle of evolvable hardware

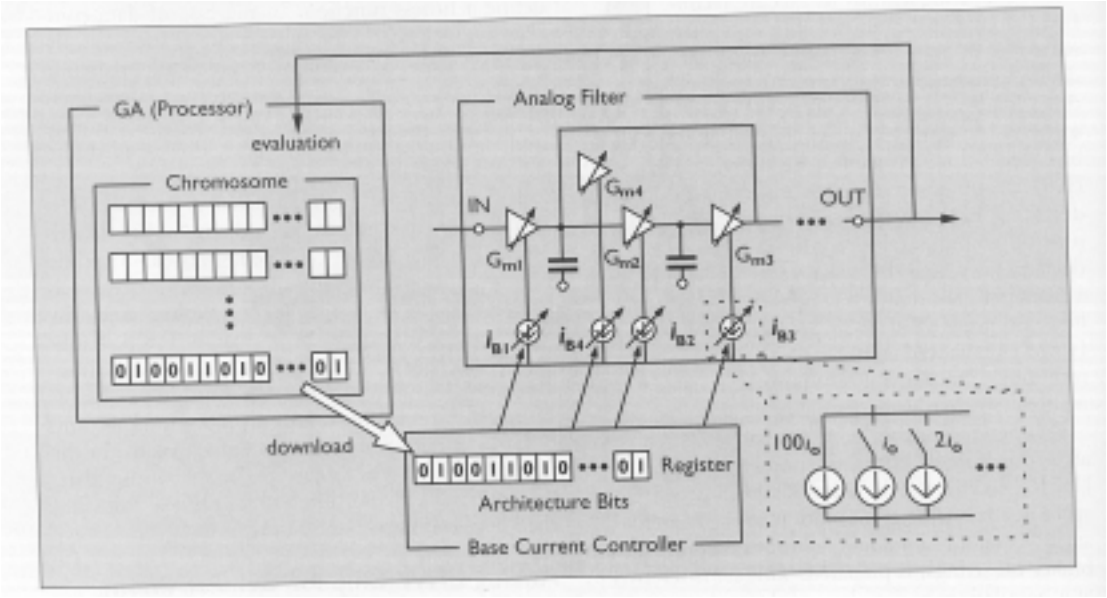


Field Programmable Gate Array (FPGA)

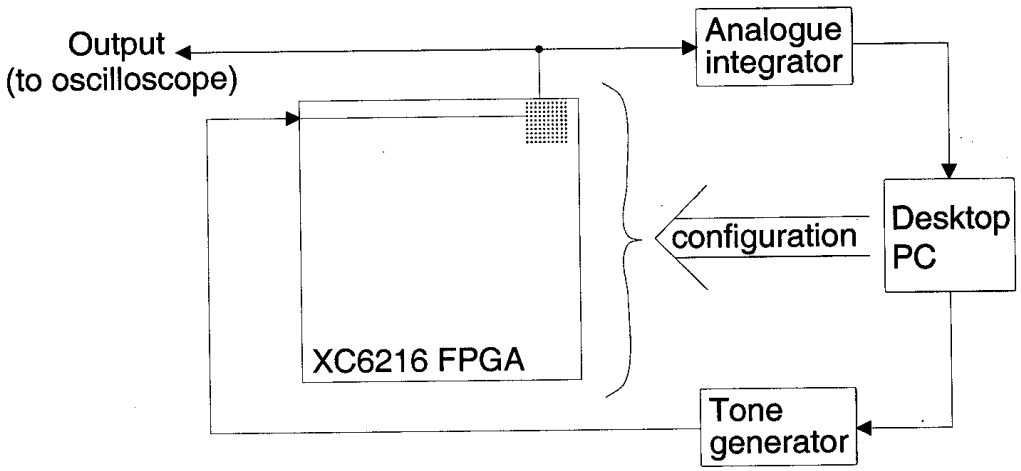
Parameters	1985	1998
Transistor width	3 um	0.25 um
Die size	25 mm2	400 mm2
Clock Frequency	20 MHz	350 MHz
Pins per package	48	630
Number of cells	64	8,464
Size of configuration bits	11,360	5,433,888
Power supply	5 volts	2.5 volts

A quick tour on EHW.

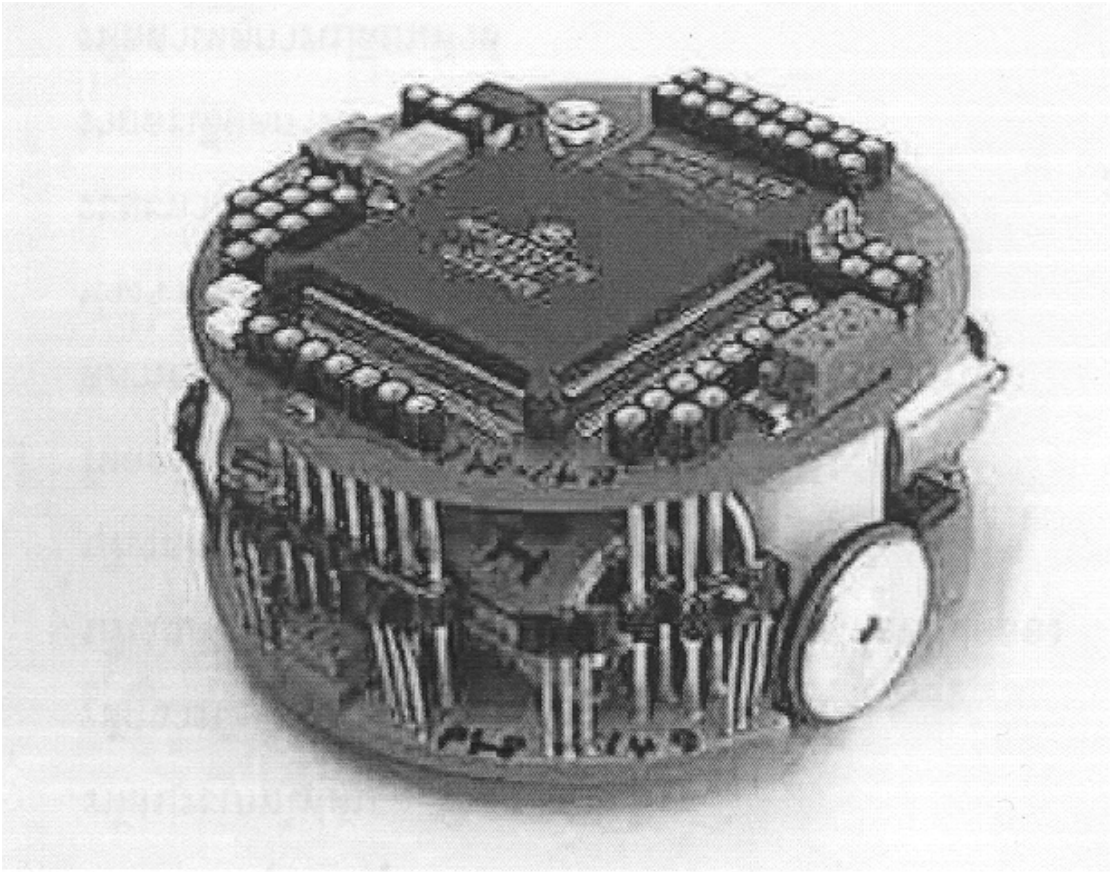
EHW as an Alternative to Electronic Circuit Design



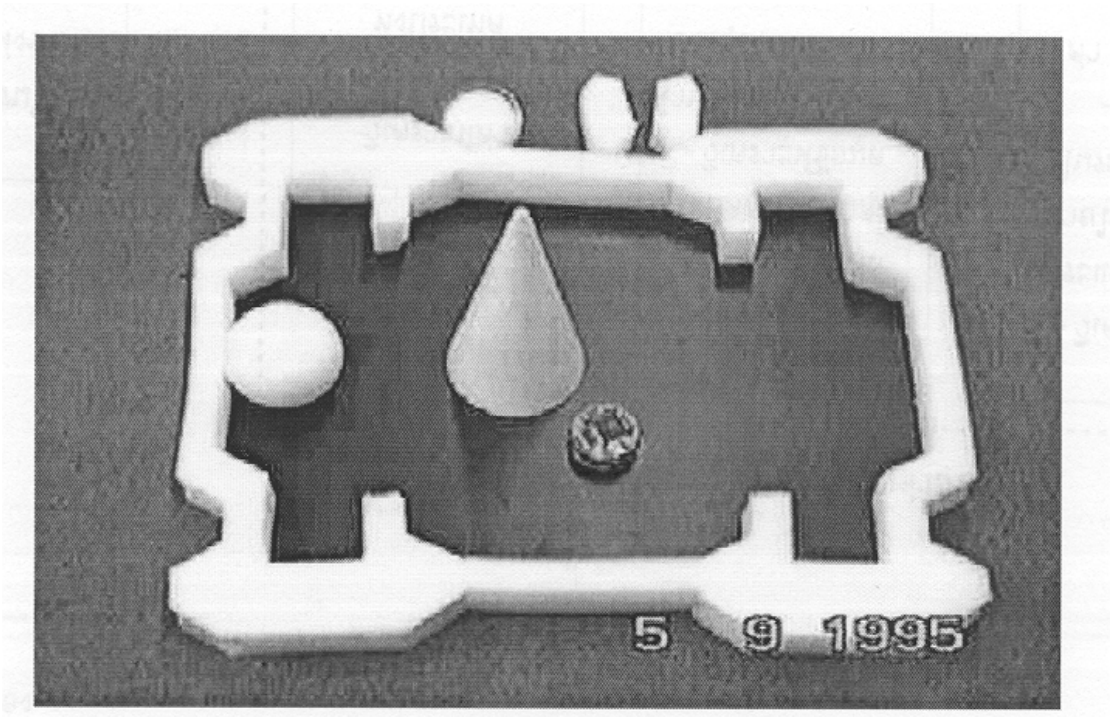
The analog EHW chip for IF filter



Evolving a frequency discriminator (Thompson, ICES 96)



A mobile robot



Evolving robot controller (Nordin, 1995)

Two Major Approaches

Early and some of the recent work related to EHW only dealt with optimisation of VLSI circuits, such as cell placement, logic minimisation and compaction of symbolic layout.

Circuit functions were not designed/evolved by EAs.

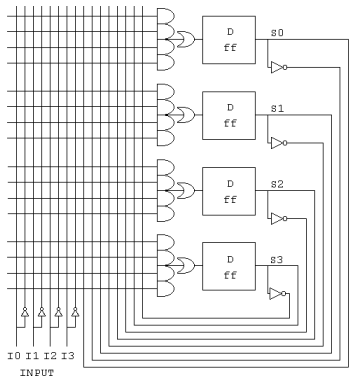
Recent work concentrates on evolving circuit architectures and thus functions. Two major approaches have been used:

1. Indirect Approach, and
2. Direct Approach

Indirect Approach to EHW Circuit Design

The indirect approach does not evolve hardware directly, but evolves an intermediate representation (such as trees) which specifies hardware circuits.

Evolving digital circuits.



For example, “Synthesis of Synchronous Sequential Logic Circuits” (Chongstitvatana, ICES’98) evolving : frequency divider, parity checker, modulo-5, serial adder. Table of GAL wiring were used to represent the circuit.

Evolving analog circuits.

For example, Koza's work on evolving a lowpass ``brick wall'' filter, an asymmetric bandpass filter, an amplifier, etc. Trees were used to represent circuits. The results were competitive with human designs

Direct Approach to EHW Circuit Design --- Gate Level

The direct approach evolves hardware circuit's architecture bits directly. It works well only with reconfigurable hardware, such as FPGA (field programmable gate array) from Xilinx.

The gate level evolution implies that the ``atomic'' hardware functional units are logical gates like AND, OR, and NOT. The evolution is used to search for different combinations of these gates.

Typical examples include XOR, counters, FSMs (Finite State Machines), multiplexors, and an electronic oscillator.

One argument for the direct approach is to exploit hardware resources by unconstrained hardware evolution.

Direct Approach to EHW Circuit Design --- Function Level

The gate level evolution runs into the scalability problem quickly.

The function level evolution uses high-level functions such as addition, multiplication, sine, cosine, etc., and thus is much more powerful.

The work is better viewed as an attempt towards adaptive hardware, rather than as a design alternative.

Advantages of Evolutionary Design

- Explores a larger design space and thus may be able to discover novel designs.
- Does not assume a priori knowledge and thus can be applied to various domains.
- Does not require exact specification and thus can design complex systems which cannot be handled by conventional specification-based design approach.
- However, constraints and special requirements could be imposed on the evolution if necessary through the fitness function and chromosome representation.
- Some analog circuits might be too difficult (or costly) to design by human experts.

Scalability of EHW

1. Scalability of the algorithm: Time complexity of the EA for EHW?

2. Scalability of the representation: Size of chromosomes vs. Size of EHW?

3. Time is more crucial since the size of chromosome (space) is usually polynomial in the size of EHW circuits.

Will Electronic Speed Solve the Scalability Problem

There have been some expectations that the speed of simulated evolution would not be a problem in a few years as faster VLSI chips come out.

This statement can be misleading. Electronic speed is not a solution to the scalability problem. The scalability problem has to be addressed at the fundamental level.

Circuit Verification/Test and Fitness Evaluation

- How to verify the correctness of EHW? How to find a fitness function which guarantee the correctness of EHW?

- For example, if all 4-bit numbers have been correctly added, would all 5-bit, 6-bit, etc., numbers be added correctly by the same circuit?

- Exploiting hardware resources is attractive. Has an EHW exploit something totally irrelevant, such as room temperature or minor Earth movement?

- Is it practical to test all possible situations in which an EHW might be used?

- How robust is EHW to minor environmental changes? Does it degrade gracefully?

- When to stop simulated evolution? How to know whether a correct circuit has been evolved?

EHW as an Adaptive System

Current work on adaptive EHW can be classified into two major categories:

1. EHW controllers.

2. EHW recognisers and classifiers.

EHW Controllers

A number of control tasks can be performed by EHW, e.g., ATM control and robot control among others.

Some examples:

- Evolving an artificial ant to follow the John Muir Trail in simulation.

- Evolving a wall following robot in a simulated environment, ``virtual reality".

- Evolving an ATM traffic shaper.

- Evolving an adaptive equaliser.

EHW Recognisers and Classifiers

Evolving FPGA to perform learning tasks, such as letter recognition, the comparator in a V-shape ditch tracer, two-spiral, Iris, FSMs, etc.

Unlike most other studies, generalisation is explicitly emphasised here.

A complexity (regularisation) term was included in the fitness evaluation function.

Other EHW-Related Work

Self-reproduction and self-repair hardware at Logic Systems Laboratory (LSL) Computer Science Department, Swiss Federal Institute of Technology -- Lausanne.

Artificial brains. CAM-BRAIN from ATR (Evolutionary Systems).

Some Challenges to Adaptive EHW

- Scalability: Efficiency of simulated evolution.
- Generalisation: Dealing with new environments.
- Disaster prevention in fitness evaluation during on-line adaptation.
- On-line adaptation: incremental evolution / learning.

Concluding Remarks

Evolutionary design of digital circuits would not be able to compete with the conventional approach.

Evolutionary design of analog circuits needs to address the issues of circuit verification and robustness.

Adaptive EHW has most potentials, but would need individual learning to implement on-line learning.

The most profitable application domains for EHW would be those which are very complex but highly specialised.