

An Interconnection Structure for Path-Delay Constrained IC Floor Plan Packing

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Abstract

This paper presents an interconnection structure, called median-line structure, for signal nets used during floor plan packing process in physical VLSI design. The structure is easily computed and closely related to the rectilinear minimum spanning tree structure. In addition, the relationship between a functional module position and its signal net delays is convex. Therefore, the path-delay constraints associated with a module can be easily converted to a continuous range of feasible positions of the module which is used during the packing process to avoid timing violation.

I. Introduction

The increasing chip size along with the decreasing device size make the physical design of VLSI circuits a very time consuming design process. In order to alleviate the physical design complexity, the design is usually divided into several successive and iterative processes. Given a structural specification and constraints from a high level synthesis process which consists of (1) a set of modules and their interconnections, (2) the sizes, estimated delays, shape constraints (for variable-shaped modules), pin positions (for fixed-shaped modules) and functionalities of the modules, (3) the expected chip aspect ratio, (4) the number of distributed I/O pads at the periphery of the chip, and (5) the timing constraints, which are the actual arrival times at the input pins and the required arrival times at the output pins, the physical design process determines the integrated circuit layout which satisfies both the geometrical and timing constraints, and minimizes the chip area. Note that in the physical design methodology presented here, there are two types of modules *fixed-shaped module* which is a pre-designed module whose exact shape, size, and I/O pin positions are known and *variable-shaped module* whose estimated area and feasible ranges of width and height are given but not yet designed in detail.

Performance-driven chip floor planning is one of the major design processes during physical VLSI design. The floor planning determines the positions and shapes of modules so that modules having a restricted timing relationship should be closely placed in order to reduce critical path delay while, if necessary, pushing some modules on less critical paths apart. In the physical

design methodology used here, the chip floor planning is divided into three successive sub-processes. First, the I/O pad assignment process maps each off-chip I/O pin of the network to one I/O pad in such a way that the subsequent placement process yields a good result [1]. Next, an initial module placement which satisfies all the timing constraints and has minimum module overlaps is determined [2]. Finally the floor plan packing process relocates, reorients, and reshapes the modules in order to reduce the chip area while satisfying the timing constraints.

In this paper, we presents an interconnection structure, called median-line structure, for signal nets used during floor plan packing process in physical VLSI design. The structure is easily computed, closely related to the rectilinear minimum spanning tree structure, and can be used in path-delay constrained design. We begin by briefly describe the overview of module and interconnection models used throughout the chip floor planning in section II. Then the median-line structure is explained in detail in section III. Section IV shows the strong correlation between the proposed model and the rectilinear minimum spanning tree. Section V presents how the proposed model supports the path-delay constrained design. And the conclusion is given in Section VI.

II. Module and Interconnection Models

In order to be able to formulate and practically solve the physical design problems, modules and interconnections, are modeled so that they are correctly represented during the design. The models are gradually modified to increase the model's accuracy as the design proceeds. In the I/O pad assignment, all modules are modeled as circles whose area equals that of the area of the associated actual module. During the initial placement process, only the variable-shaped modules are modeled as circles whereas the exact shapes and sizes of the fixed-shaped modules are used. During the floor plan packing, the shapes of the variable-shaped modules are deformed to globally minimize chip area. Therefore, all the modules are modeled as their exact shapes and sizes including the routing channel areas surrounding the modules which can be pre-computed and periodically updated as presented in [3, 4].

For the interconnection structure, the shortest boundary distance between any two circles represents the interconnection length between the two corresponding modules in the I/O pad assignment. A *net-node* interconnection structure module is used during the initial placement process, where each net is represented by a node from where every terminal of that signal has to connect. During the floor plan packing, the node representing the signal is turned into a line (called *median-line*) from where every terminal of the signal has to connect either vertically or horizontally. Note that the actual lengths of signal nets are not yet known until all the modules are placed and the detailed routing is completed. However, the interconnection structure model presented above provide the estimated net lengths in such a way that the relative lengths among signal nets are likely to be closely the same as the relative actual lengths after final routing.

III. Median-line Interconnection Structure

An interconnection structure called the median-line structure is used for the net length estimation during floor plan packing (see Figure 1). The *horizontal* median-line of signal s is defined to be a line connecting (xl_s, ym_s) to (xr_s, ym_s) where xl_s and xr_s are the left- and right-most position among the terminals of signal s , and ym_s is the position of the terminal of signal s which equally (or almost equally) partitions the terminals of signal s into upper and lower sides of the line, that is, the line is located at the median position among the signal terminals. The *vertical* median-line of signal s is defined similarly to be a line connecting (xm_s, yb_s) to (xm_s, yt_s) . Connecting a signal net s is done either by connecting the terminals to the vertical median-line of the signal using horizontal lines (Figure 1a) or by connecting the terminals to the horizontal median-line of the signal using vertical lines (Figure 1b) whichever shorter in total length.

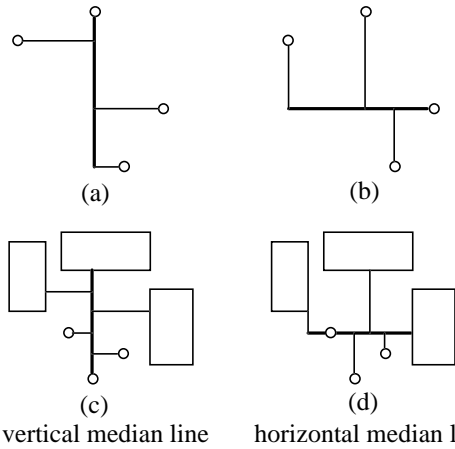


Figure 1. Median-line interconnection structure.

The above definition of the median-line structure is only applicable for signal nets all of whose terminals belong to fixed-shaped modules. Since the position of

any signal terminal of a variable-shaped module is not yet determined at this stage, it can be at any location of the boundary of its corresponding module. Therefore we need to modify the definition of the median-line to cover for terminals of variable-shaped modules. This is done by extending the definition of the two end-points of the median-lines as follows.

$$xl_s = \min \left\{ \min_{z \in Zf_s} \{x_z\}, \min_{z \in Zv_s} \{Right(m_z)\} \right\}$$

$$xr_s = \max \left\{ \max_{z \in Zf_s} \{x_z\}, \max_{z \in Zv_s} \{Left(m_z)\} \right\}$$

where Zf_s is a set of terminals of signal s which belong to fixed-shaped modules, Zv_s is a set of terminals of signal s which belong to variable-shaped modules, and m_z is the module corresponding to signal terminal z . For the ym_s , let first define $T(s, ym_s)$ to be a set of fixed-shaped module terminals of signal s which are above ym_s including a set of terminals of signal s belonging to variable-shaped modules whose bottom sides are above ym_s . $B(s, ym_s)$ is defined similarly to be a set of fixed-shaped module terminals of signal s which are below ym_s including a set of terminal of signal s belonging to variable-shaped modules whose top sides are below ym_s .

$$T(s, ym_s) = \{z | y_z > ym_s, z \in Zf_s\} \cup \{z | Bottom(m_z) > ym_s, z \in Zv_s\}$$

$$B(s, ym_s) = \{z | y_z < ym_s, z \in Zf_s\} \cup \{z | Top(m_z) < ym_s, z \in Zv_s\}$$

So, the y-coordinate of the horizontal median-line is the ym_s which has the difference in the number of elements in $T(s, ym_s)$ and in $B(s, ym_s)$ not more than one. Therefore, the interconnection length of net s using the median-line structure is

$$l_s = \min \{lh_s, lv_s\}$$

$$lh_s = (xr_s - xl_s) + \sum_{z \in Zf_s} |y_z - ym_s|$$

$$+ \sum_{z \in Zv_s \cap T(s, ym_s)} (Bottom(m_z) - ym_s)$$

$$+ \sum_{z \in Zv_s \cap B(s, ym_s)} (Top(m_z) - ym_s)$$

$$lv_s = (yt_s - yb_s) + \sum_{z \in Zf_s} |x_z - xm_s|$$

$$+ \sum_{z \in Zv_s \cap R(s, xm_s)} (Left(m_z) - xm_s)$$

$$+ \sum_{z \in Zv_s \cap L(s, xm_s)} (Right(m_z) - xm_s)$$

IV. Median-Line vs. RMST

Since the net routes are not yet determined at the floor planning step, net length based on an interconnection structure may not accurately represent

the actual net length after routing. However, net length estimation using the median-line structure provides sufficient relative lengths among signal nets. Figure 2 shows the results of a set of experiments which demonstrate the correlations of total net lengths using rectilinear minimum spanning tree (RMST), using the median-line structure model, and using the widely used half-perimeter model (1/2P)* [5-8]. The plots show that both the median-line and the 1/2P models have strong correlations with the RMST model. The same correlation between the RMST and 1/2P models was also shown in [9]. However, the median-line structure provides a better net length estimation than the 1/2P model. Notice from the plots that the ratio of the net lengths using the RMST and the median-line model is closer to 1 than the ratio of the net lengths using the RMST and the 1/2P. This is because any signal terminal located inside the bounding box does not contribute to any change in net length using the 1/2P model.

V. Path-Delay Constrained Packing

In the floor plan packing process, the objective is to minimize chip area while satisfying the given timing constraints. The packing operations we used are relocating modules, reorienting fixed-shaped modules, and reshaping variable-shaped modules. If module's shape and position are arbitrarily changed, it may cause timing violation. Therefore, the new shape and position of the module are temporarily set and an incremental timing analysis is performed. If there is no violation, the new shape and position are accepted, otherwise the original shape and position are restored and the packing operation fails which causes the packing procedure to try other alternatives §.

In order to avoid or lessen the number of trial and error iterations mentioned above, feasible positions of a module satisfying timing constraints can be determined. Given a module i , its feasible positions are the positions which satisfy 1) the delay constraints of all of the paths passing through the module and 2) the delay constraints of all of the multi-terminal nets connected to input terminals of module i . For the example shown in Figure 3 assume that only module i can be freely moved horizontally. Then the feasible positions of the x -coordinate of module i are the positions which satisfy the following conditions.

$$\begin{aligned} d_1 + d_3 &\leq Tr_c - Ta_a - D_p \\ d_1 + d_4 &\leq Tr_d - Ta_a - D_p \\ d_2 + d_3 &\leq Tr_c - Ta_b - D_q \\ d_2 + d_4 &\leq Tr_d - Ta_b - D_q \\ d_1 &\leq Tr_e - Ta_a \end{aligned}$$

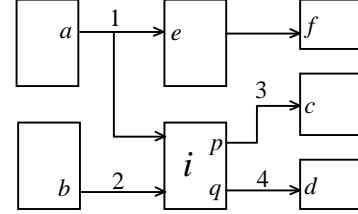


Figure 3. Example showing signal path and signal net constraints associated with module i .

where d_s is the delay time of signal s , Tr_z is the required arrival time at terminal z , Ta_z is the actual arrival time at terminal z , and D_z is the output module delay time at terminal z . Tr_z and Ta_z of all the terminals are determined by performing timing analysis. The first four conditions are the path delay constraints which take care of the delay constraints for the paths pass through the module, and the last condition is the net delay constraint which takes care of the delay constraint for the other paths which do not pass through the module, but have the net on their paths. That is, changing delay of net 1 by moving module i may violate the timing of path passing terminal a and e . Note that if the relationship between the net delays and the module position is a convex function, the feasible position of the module based on the timing constraints in a convex set (a range of positions) where the minimum and maximum positions of the feasible position set are the two positions which yield zero path delay slack.

Suppose that terminal z is connected to signal net s , z belongs to module i and module i is being relocated. In order to provide the convexity relationship between the delay of net s and the position of module i , all connection segments of signal s are fixed except the connection segment to terminal z during the movement of module i . Figure 4 shows the relationship when module i is being moved in parallel or perpendicular to the median line of signal s . If module i is a fixed-shaped module and the relative position of terminal z to the center of module i is (X_z, Y_z) , the relationships are shown in Figure 4a and 4b. If module i is a variable-shaped module with height H_i and width W_i , the relationships are shown in Figure 4c and 4d. Note that the net length estimation during module movement is not always equal to the minimum net length using the median-line structure. However, the estimation provides the convexity relationships and the net length is never underestimated. Therefore, the timing constraints are guaranteed to be satisfied when the maximum or minimum module position from the feasible module position set is chosen.

* In 1/2P, the total net length of a net equals half the perimeter of the bounding box of all the terminals of the net.

§ Details of the packing procedure is not presented here in this paper.

VI. Conclusion

An interconnection structure for signal nets used during floor plan packing process in physical VLSI design is presented. The structure is easily modeled and associated signal net lengths are easily computed. It was experimentally shown that the structure provides better estimations of net lengths than those derived using the half-perimeter model and is closely related to the rectilinear minimum spanning tree. In addition, the relationship between a functional module position and its signal net delays is convex. Therefore, the path-delay constraints associated with a module can be converted to a continuous range of feasible module position which can be used during the packing to avoid timing violation.

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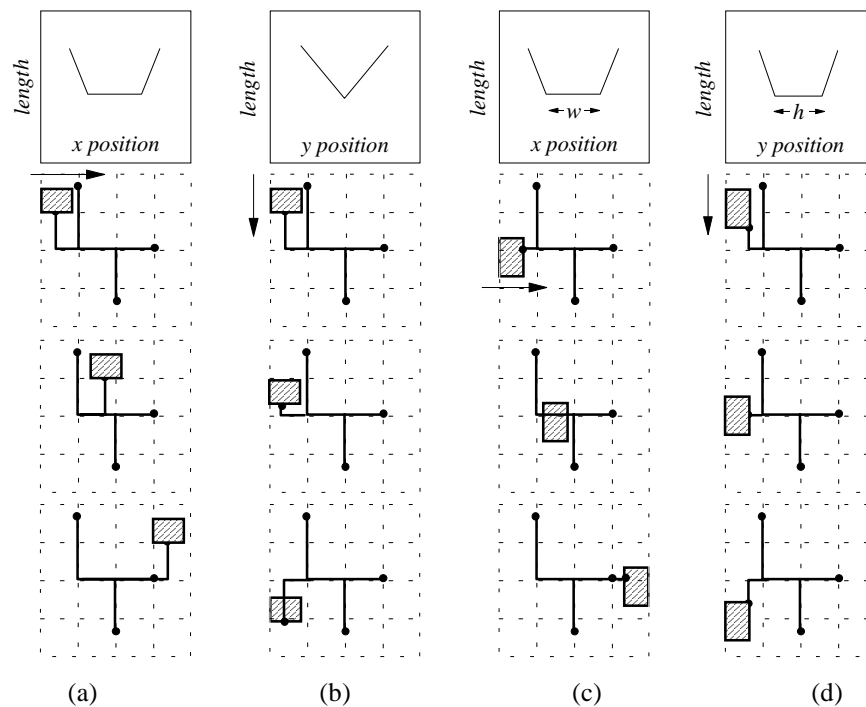


Figure 4. Plots showing net length versus module position,
(a),(b) fixed-shaped module, (c),(d) variable-shaped module