# DESIGN FOR TESTABILITY

**Somchai Prasitjutrakul**

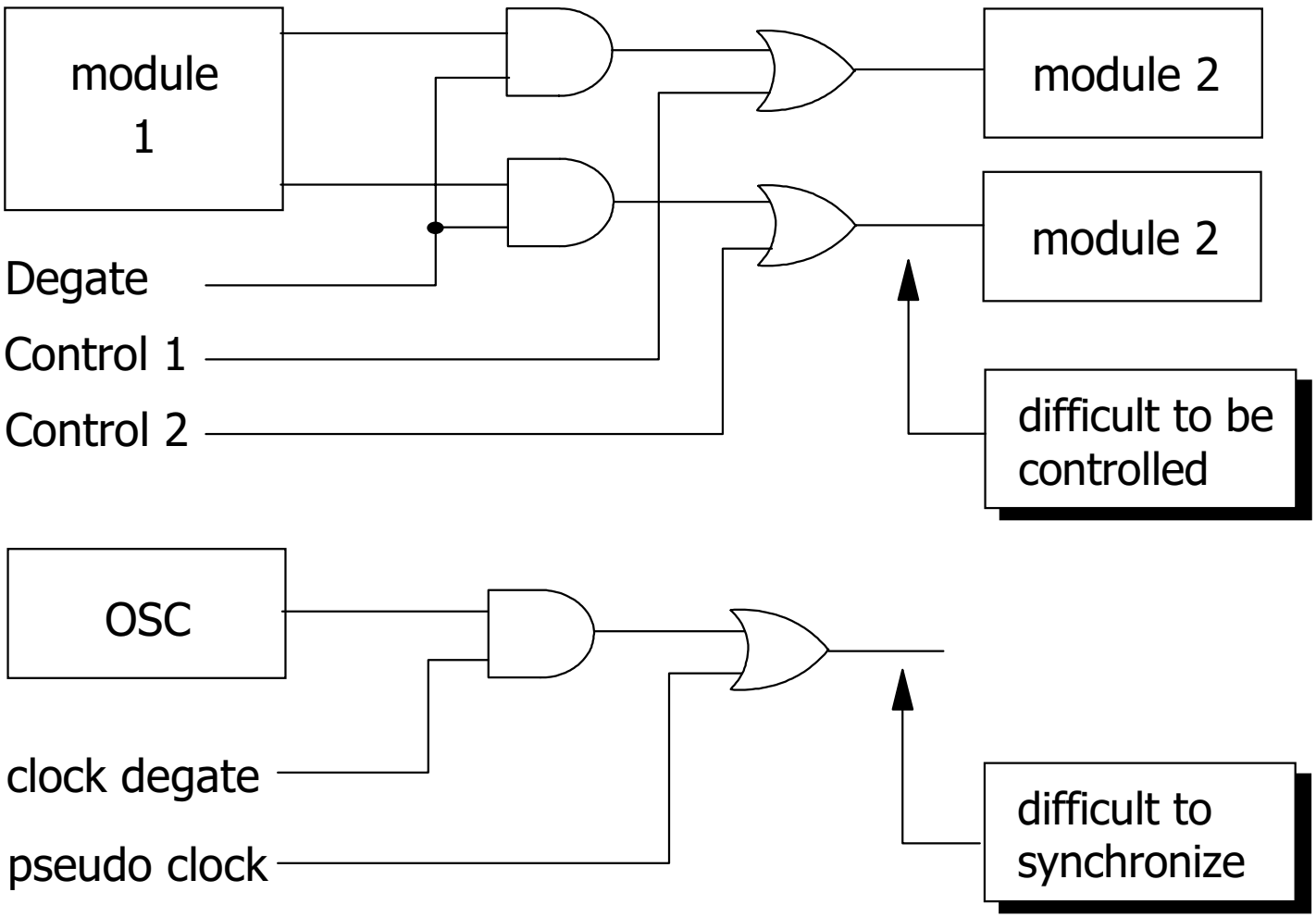
# Design for Testability

- Controllability
  the ability to eatablish a specific signal value at each node in a circuit by setting values on the circuit's inputs
- Observability
  the ability to determine the signal value at any node in a circuit by controlling athe circuits' inputs and observing its outputs

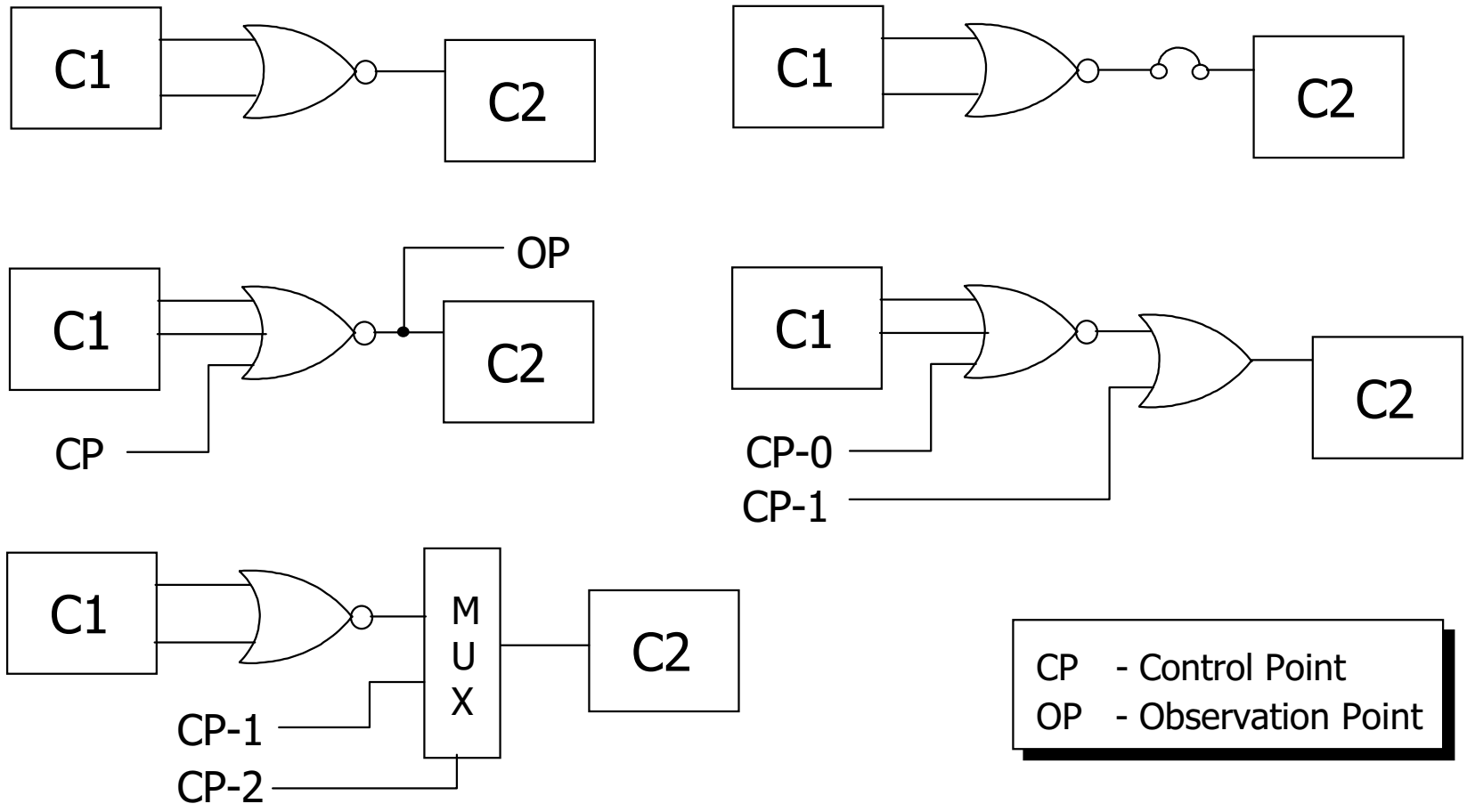
# Design for Testability

- Ad hoc techniques
  - applied to a given product
  - lower cost
- Structured approaches
  - solve the general sequential problem
  - lend themselves more easily to design automation

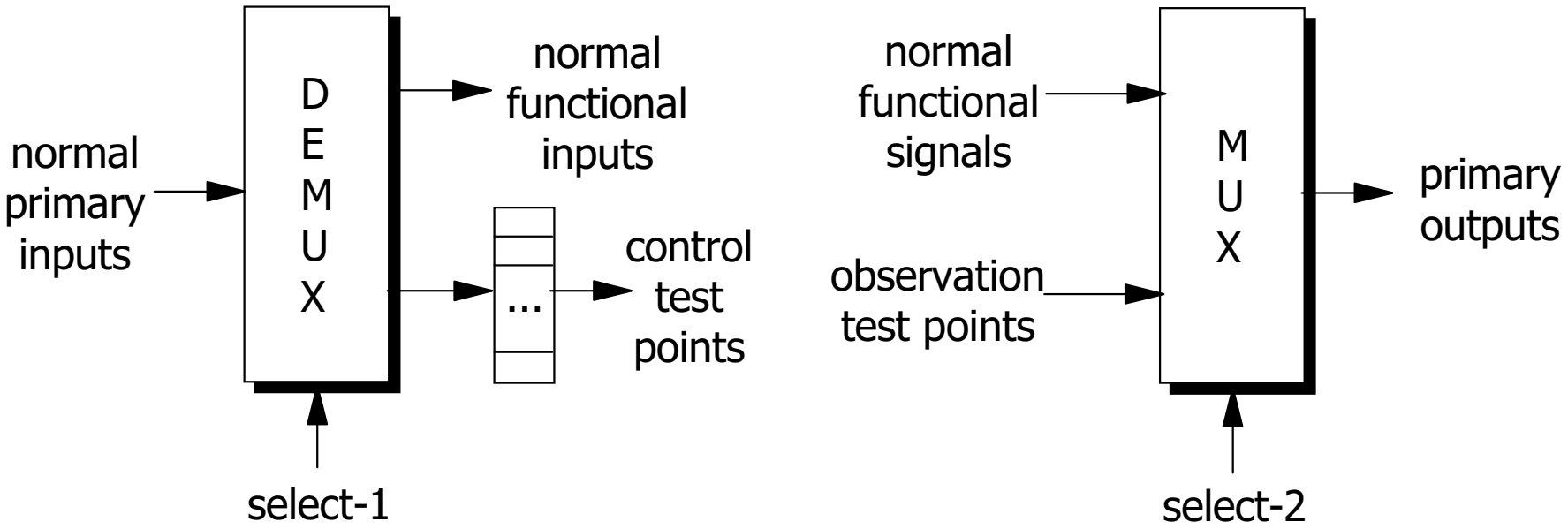
# Test Points


module
1
module 2
module 2
Degate
Control 1
Control 2
difficult to be
controlled
OSC
clock degate
pseudo clock
difficult to
synchronize

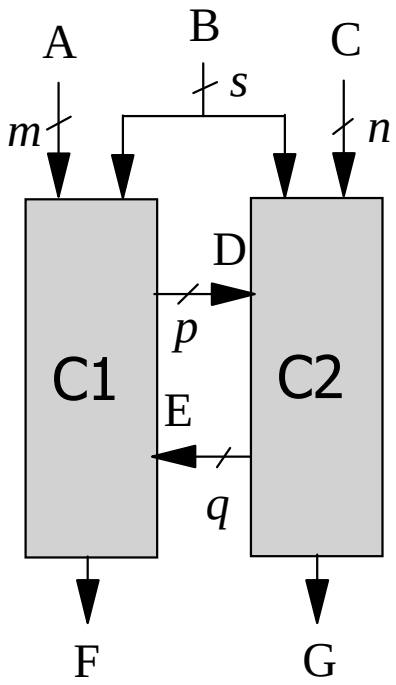
# Test Points

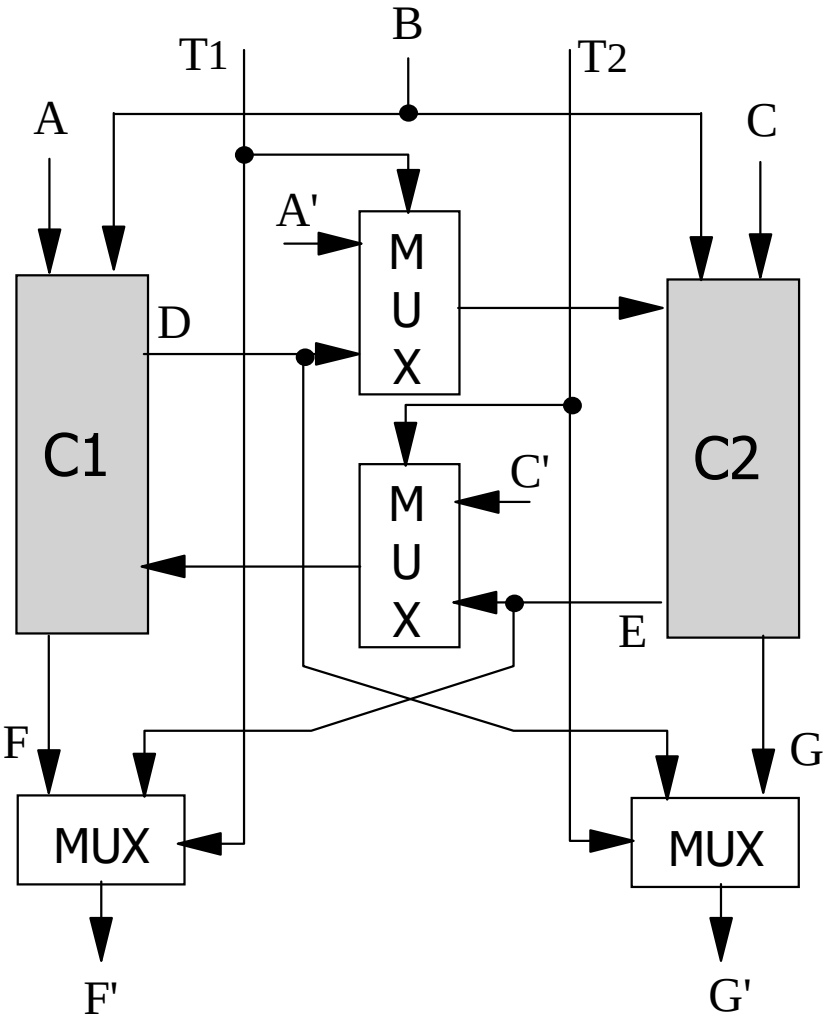

C1
C2
C1
C2
OP
C1
C2
CP
C1
C2
CP-0
CP-1
C1
M
U
X
C2
CP-1
CP-2
CP - Control Point
OP - Observation Point

# Time-Sharing I/O Ports

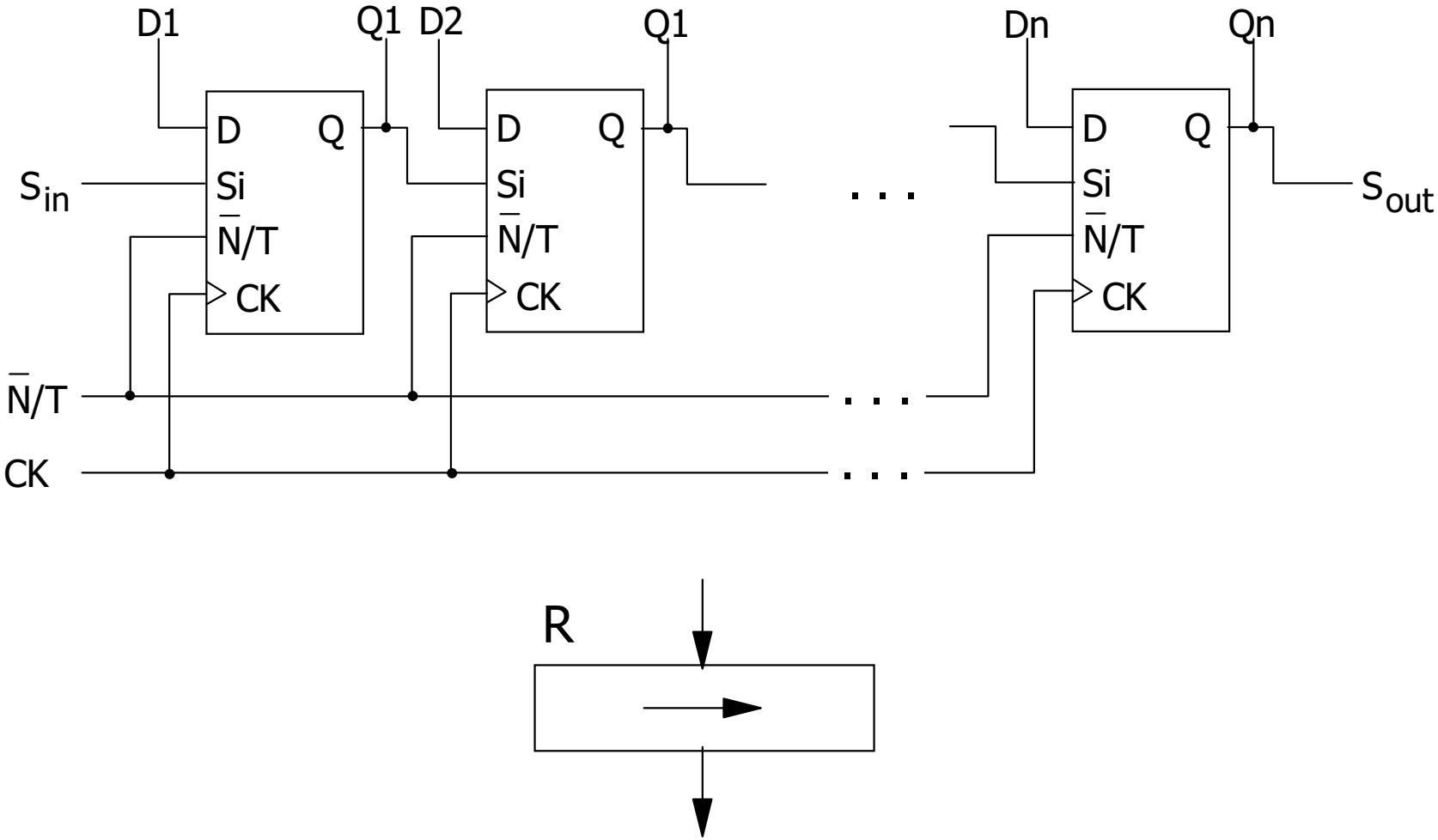


# Partitioning

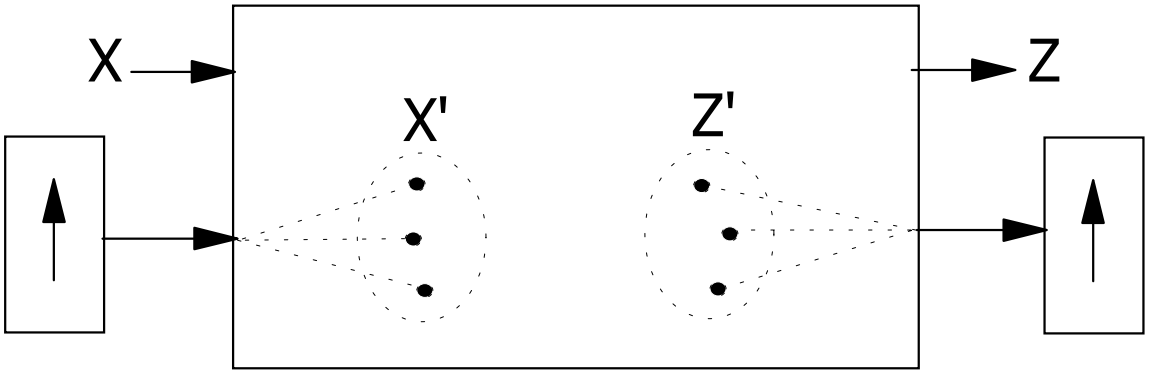


# Scan Registers



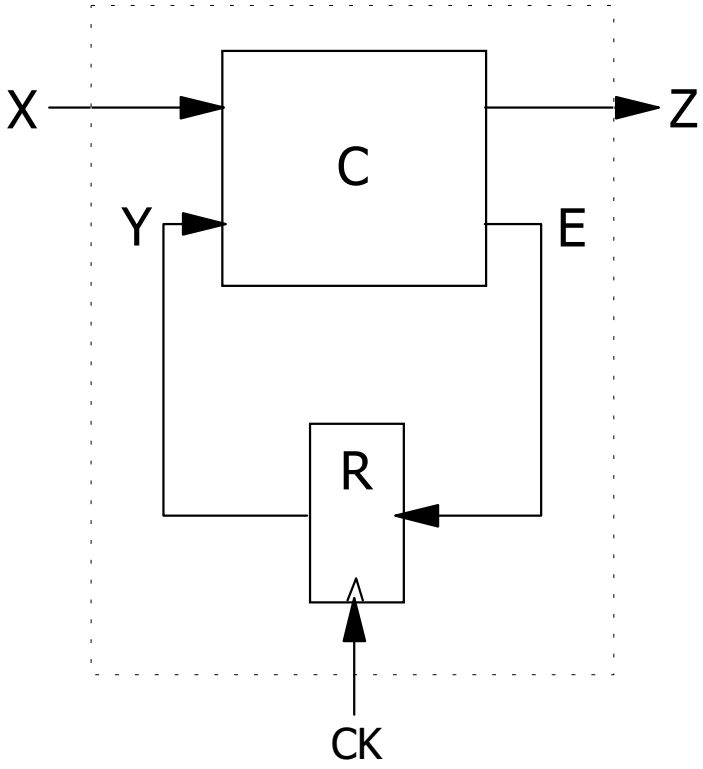
# Test Points & Scan Registers

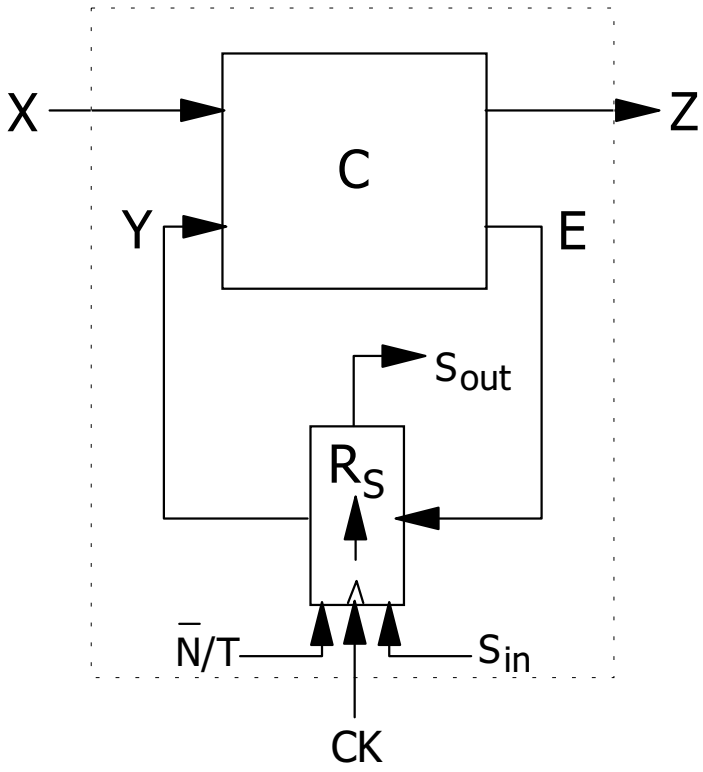


# Structured Design for Testability

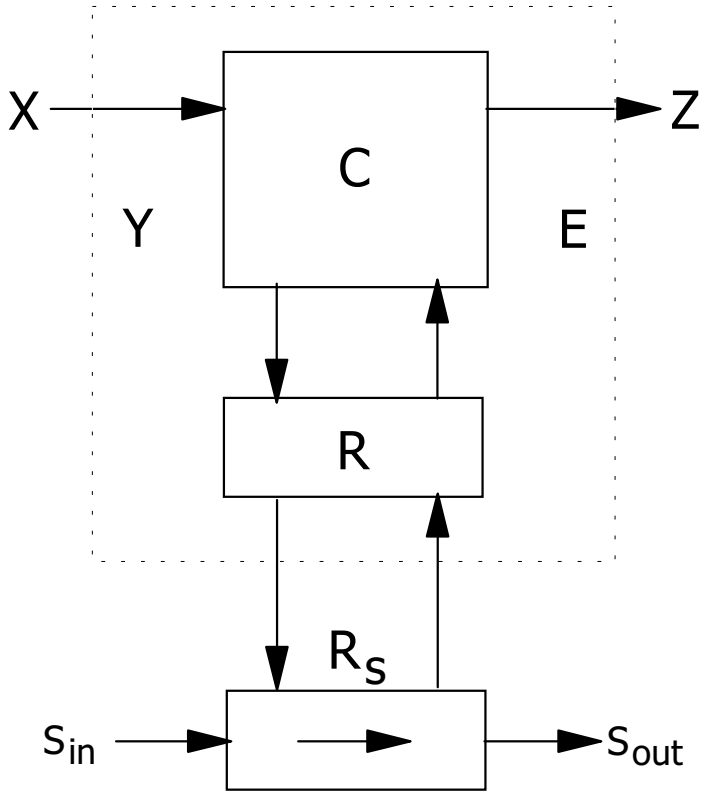
- Scan-Based Design
  - Serial Integrated Scan
  - Isolated Serial Scan
  - Random-Access Scan

# Full Serial Integrated Scan



# Isolated Serial Scan (Scan/Set)



# Random-Access Scan