Introduction to ASIC Designs

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Application-Specific IC (ASIC)

- a means to reduce
  - size
  - power
  - complexity
  - cost
- and increase
  - speed
  - functionality
  - reliability

ASIC Economics

ASIC Cost :

For N units, the overall unit cost will be :

$$\frac{\text{NRE}}{\text{N}} + \text{unit cost}$$

The value of an ASIC is :

Sum of cost of components replaced

+ Board area, complexity and drilling saved

+ Component assembly costs saved

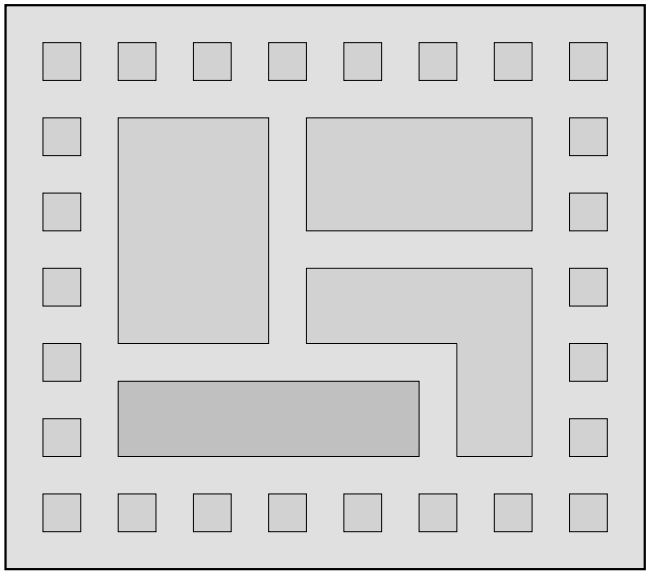
+ Power supply and cooling saved

ASIC Technologies

- Full Custom
- Standard Cell
- Gate Array
- User Configurable Arrays

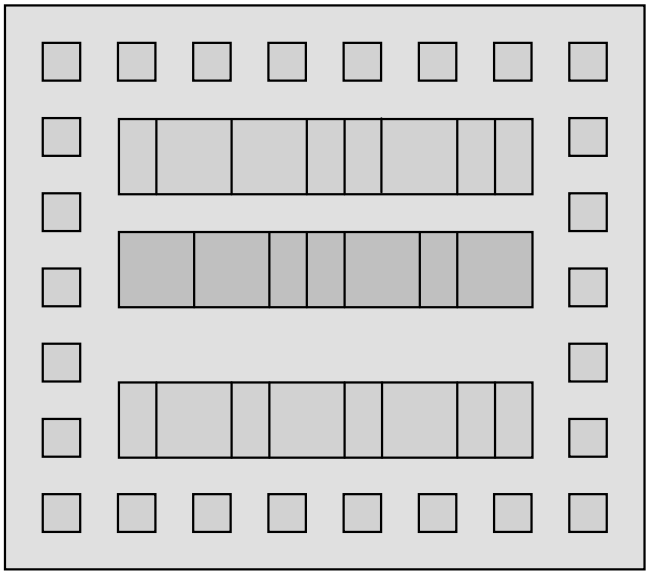
Full Custom Designs

- Highest performance
- Smallest chip area
- Highest development cost
- Longest lead time



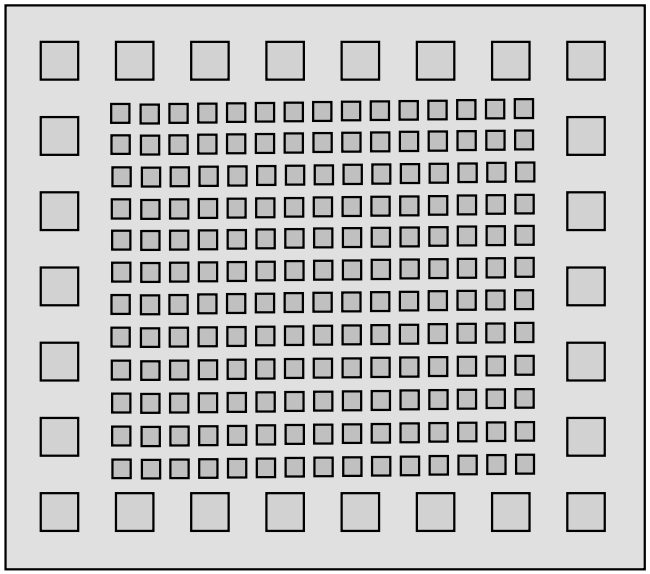
Standard Cell Designs

- Good area utilization
- High NRE
- Moderate lead-time
- High performance
- High probability of success



Gate Array Design

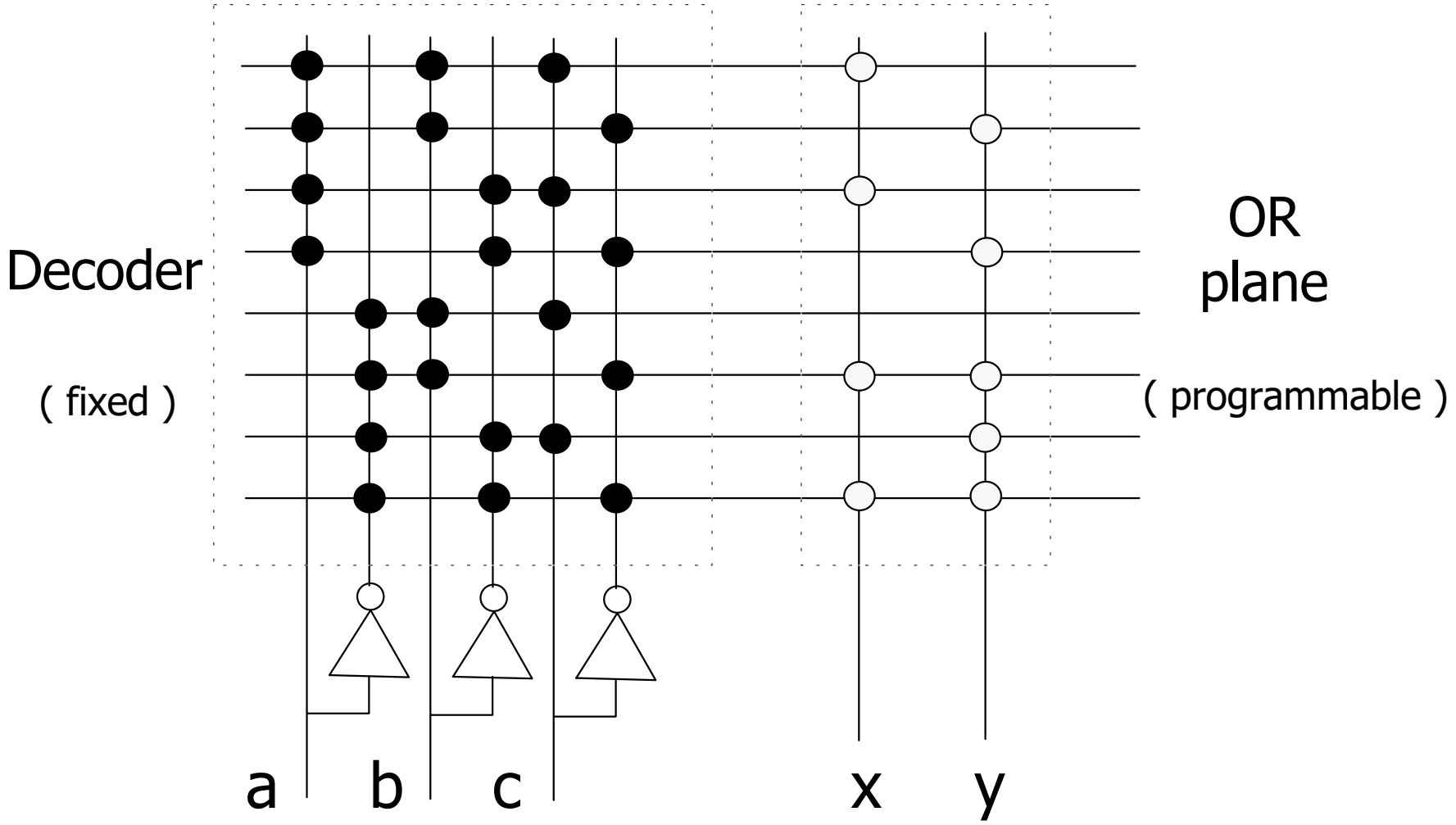
- Fewer custom masks
- Lower NRE
- Lower lead-time
- Poor area utilization
- High probability of success



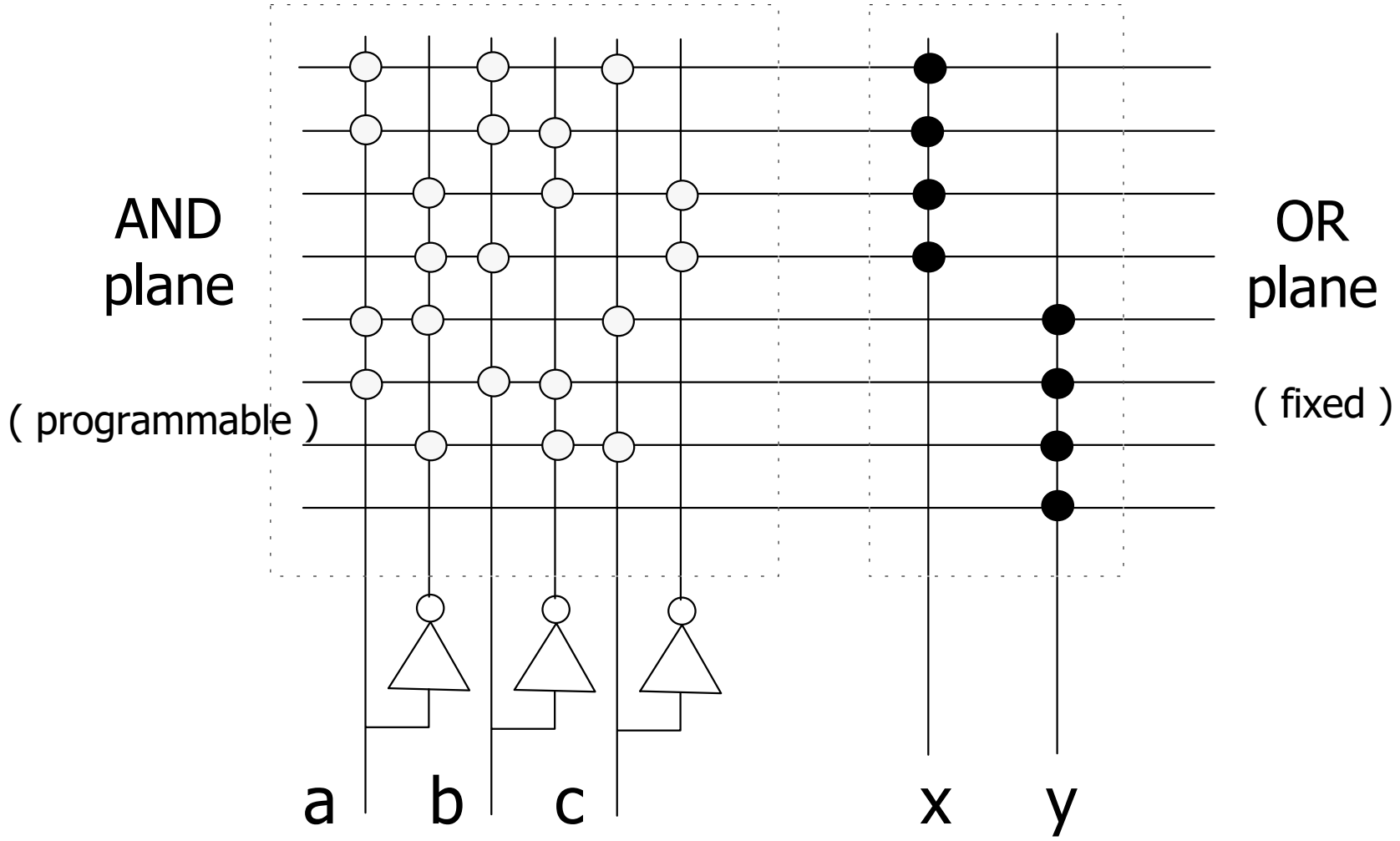
User Configurable Arrays

- FPLA (Field Programmble Logic Array)
- PAL (Programmable Array Logic)
- EPLD (Erasable Programmable Logic Device)
- LCA (Xilinx Logic Cell Array)

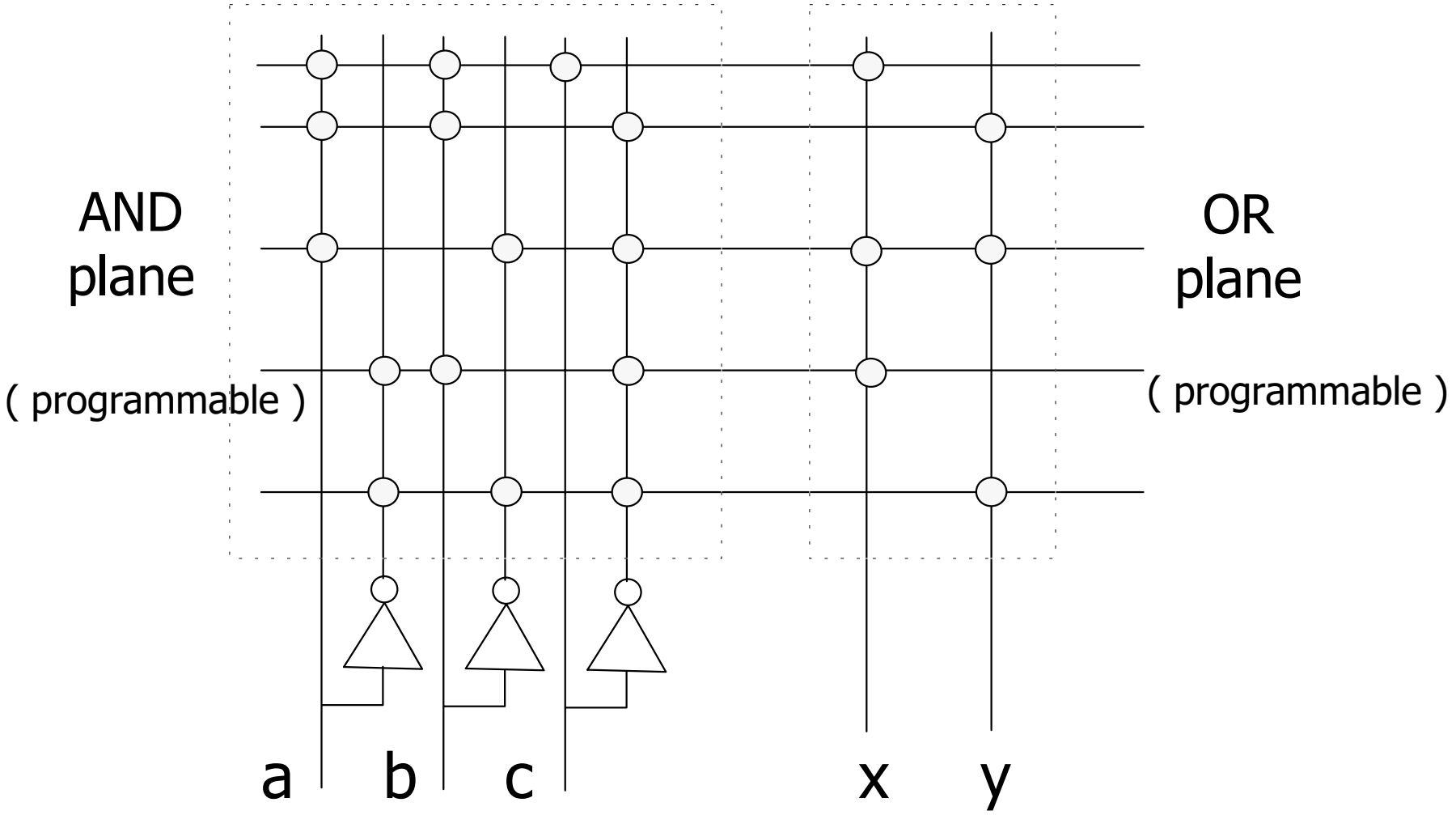
Read Only Memory (ROM)



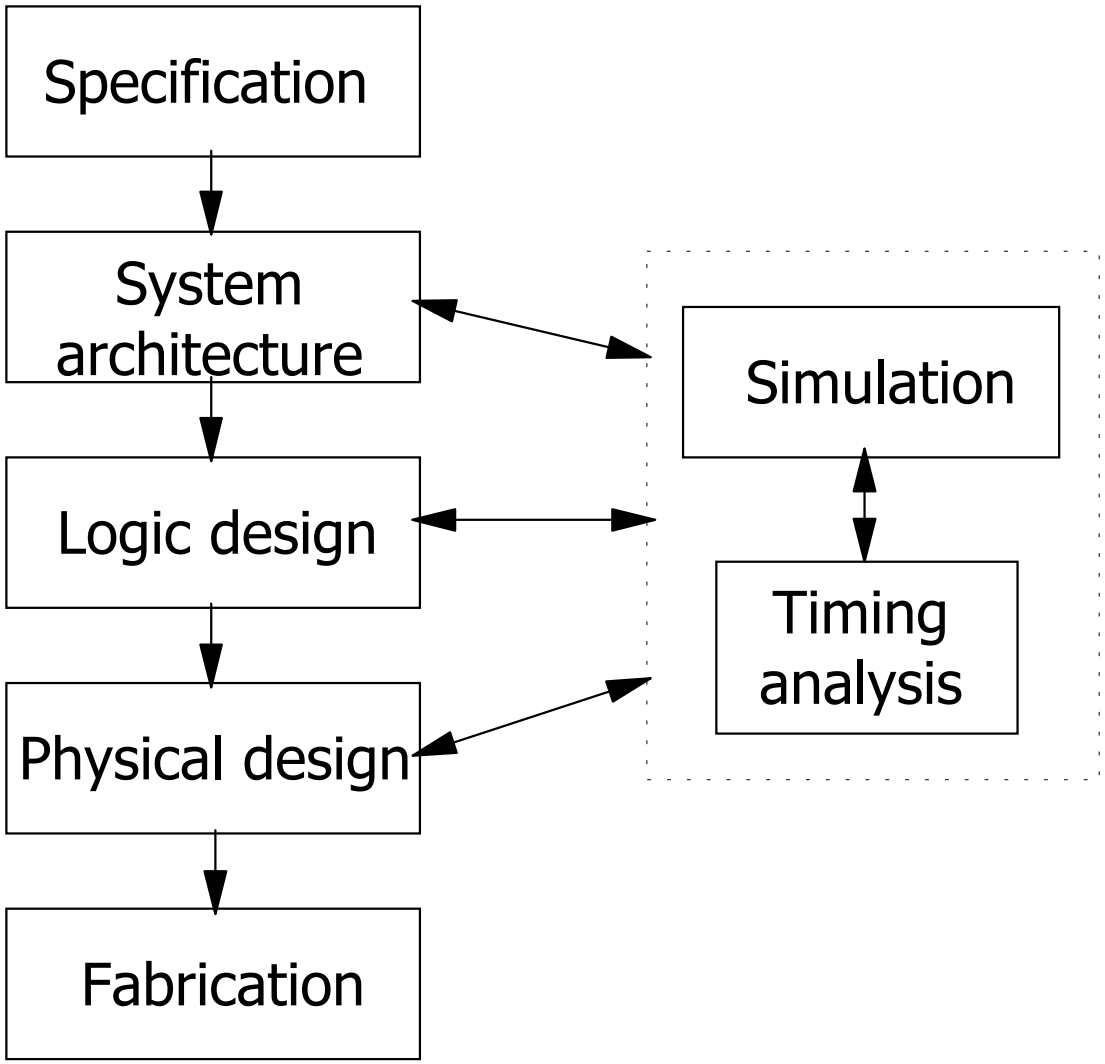
Programmable Array Logic (PAL)



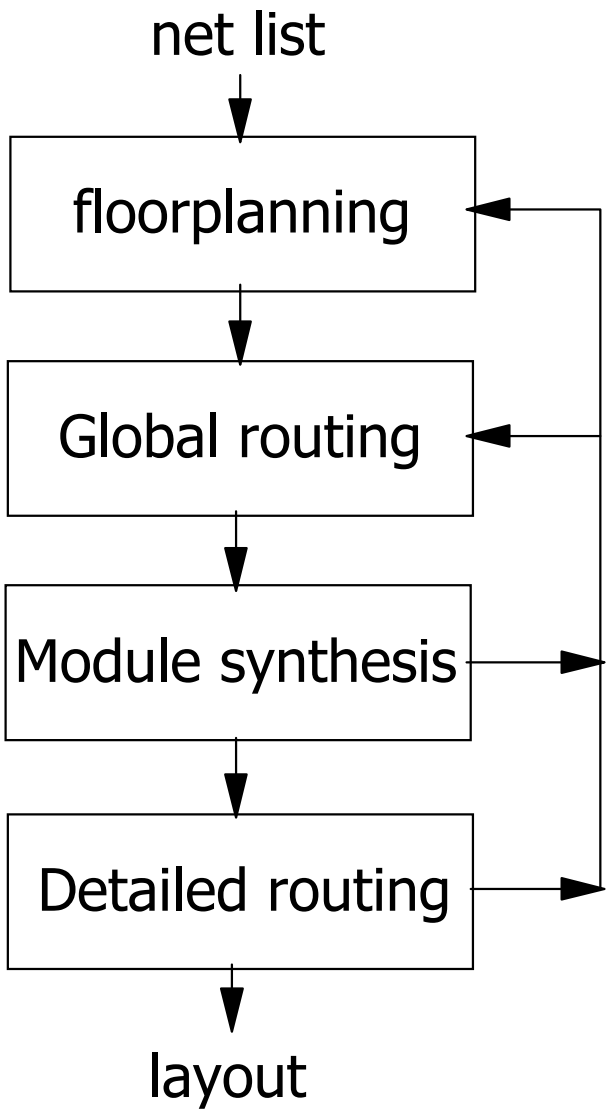
Programmable Logic Array (PLA)



VLSI Design Processes



VLSI Physical Design Processes

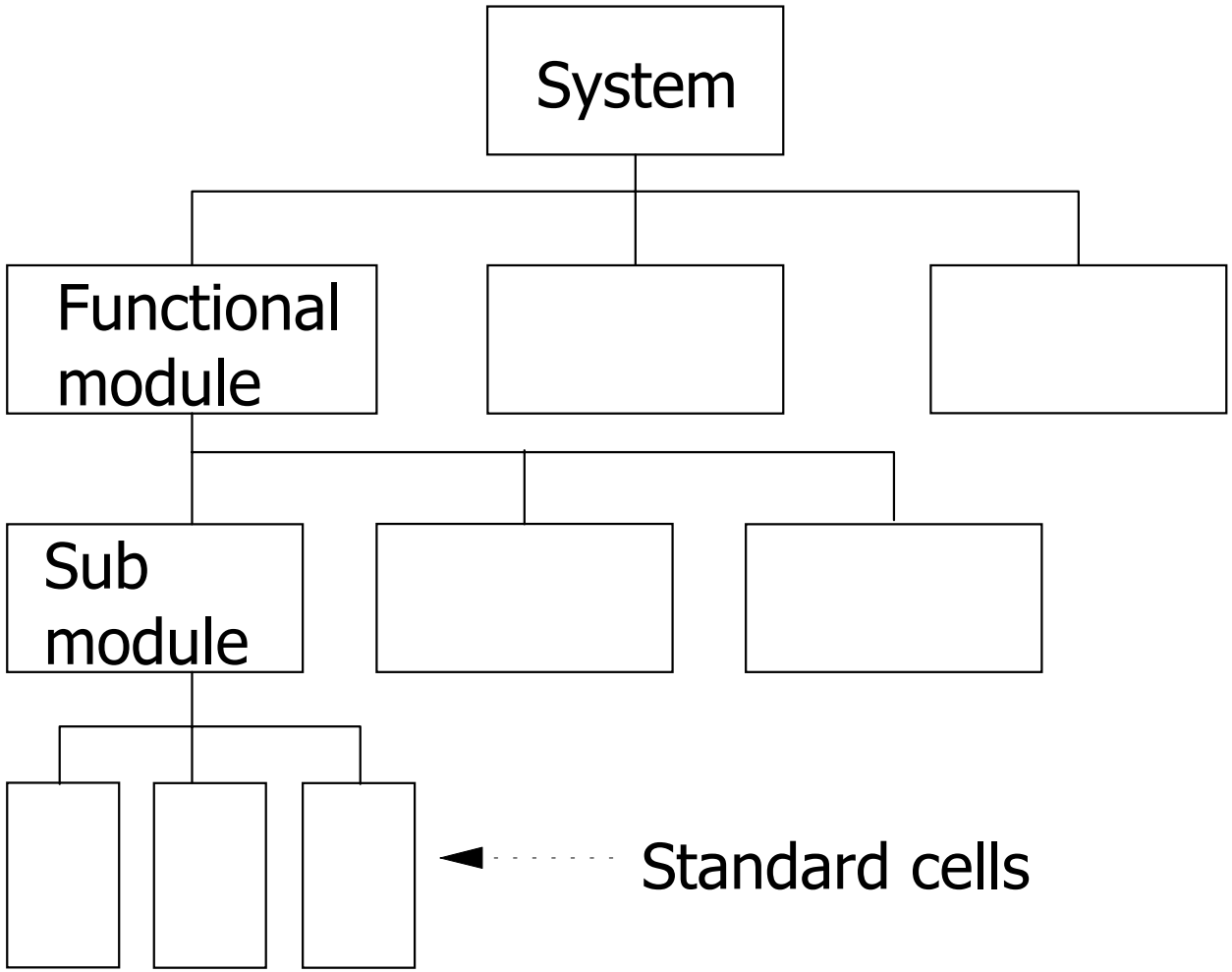


S. Prasitjutrakul 1992

ASIC Design Methodology

- Key issues in ASIC designs
  - Correctness (hierachical design)
  - Testability (design for testability)

Hierarchical Designs



Partitioning

- Functional decomposition
- Packaging convenience
- Test convenience
- Other guidelines :
  - minimum interconnection
  - testing accessibility
  - logical consistency
  - optimum cost for given production quality
  - multiple use product

Complex .vs. Simple IC Chips

- Complex chips take longer to
  - Design
  - Verify
  - Prepare test vectors for test
- Two small chips will generally yield better than one large one

Simulation

- Essential in ASIC design
  (need to get working chips the first time)
- Objectives :
  - confirm logic of design
  - confirm schematic entry correct
  - verify correct timing
  - provide reference for production testing